

Revision : 3.0

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25	ALC889

[illegible]

Model Name:GA-880GA-UD3H

Component value change history

Version: 3.0

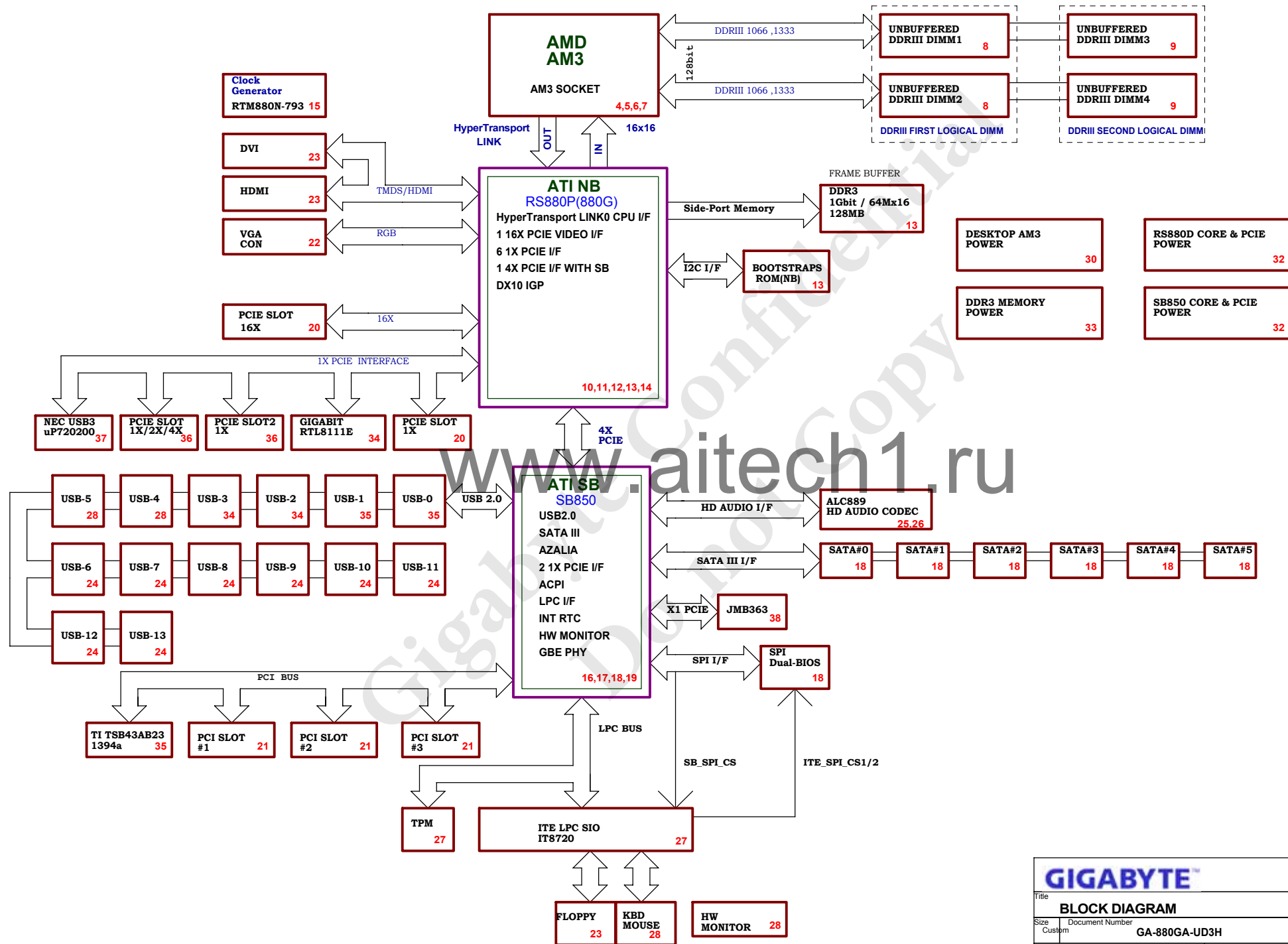
P-Code: U98144-0

[illegible]

Circuit or PCB layout change for next version

[illegible]

RS880 CUSTOMER DESKTOP REFERENCE DESIGN



GIGABYTE

Title **BLOCK DIAGRAM**

Size Custom Document Number **GA-880GA-UD3H** Rev **3.0**

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L0_CADIN_L[0..15] <L0_CADIN_L[0..15] 10
L0_CADIN_H[0..15] <L0_CADIN_H[0..15] 10
L0_CADOUT_L[0..15] <L0_CADOUT_L[0..15] 10
L0_CADOUT_H[0..15] <L0_CADOUT_H[0..15] 10



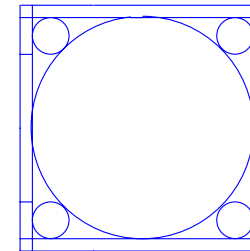
CPU-SK941AM3/S/GF[10SC1-A01941-01R]

CPU_VDD_RUN = VCORE
CPU_VDDA_RUN = VDDA25
VLDT_RUN = VCC12_HT
CPU_VDDIO_SUS = DDR15V
CPU_VDDR = CPU_VDDR12

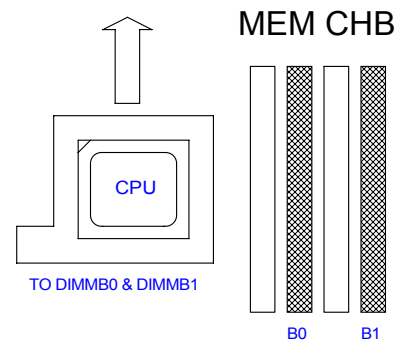
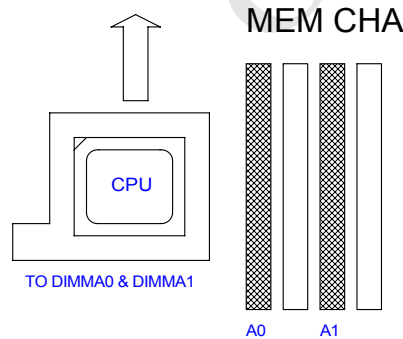
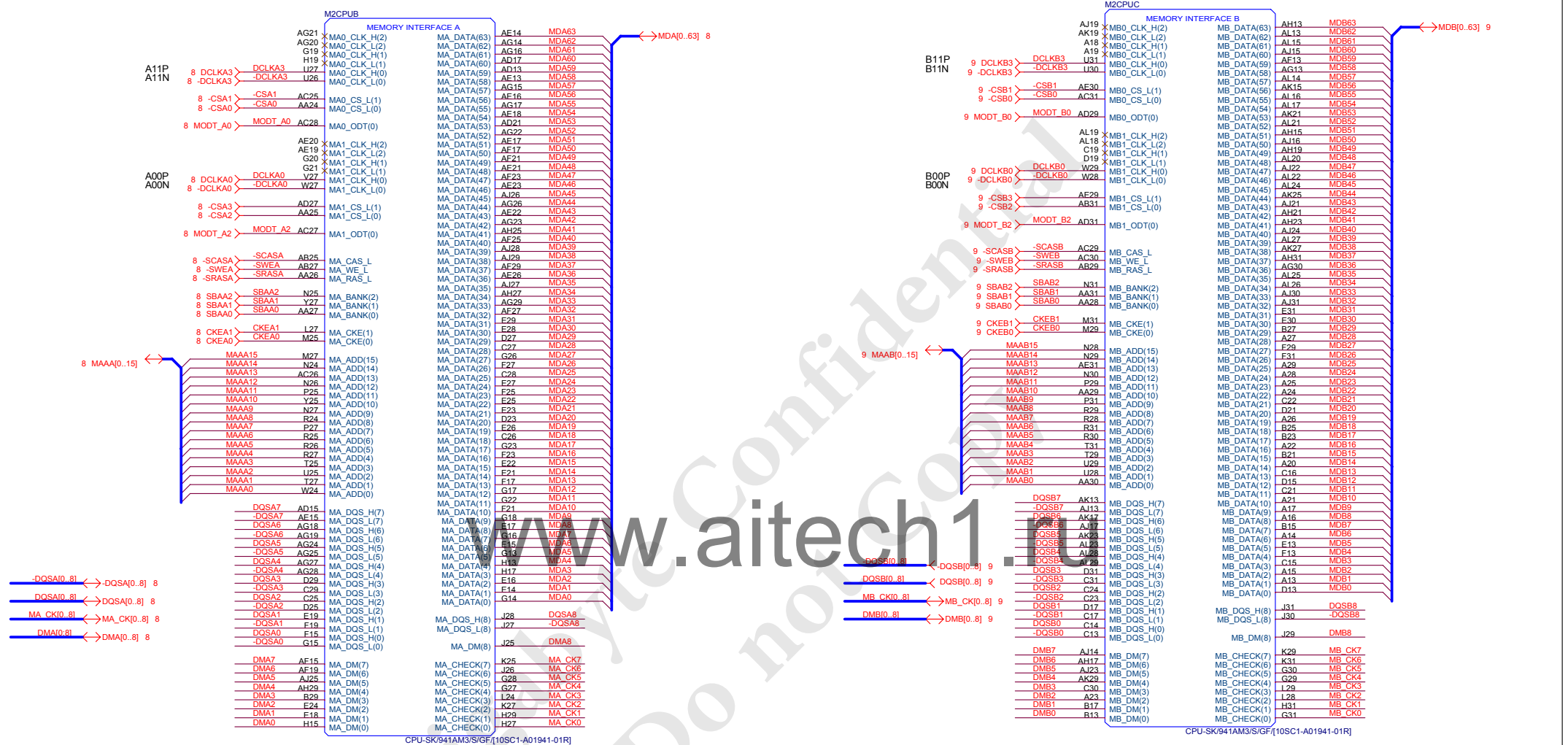
VLDT_A = VCC12_HT
VLDT_B = HT12B

M2CPU

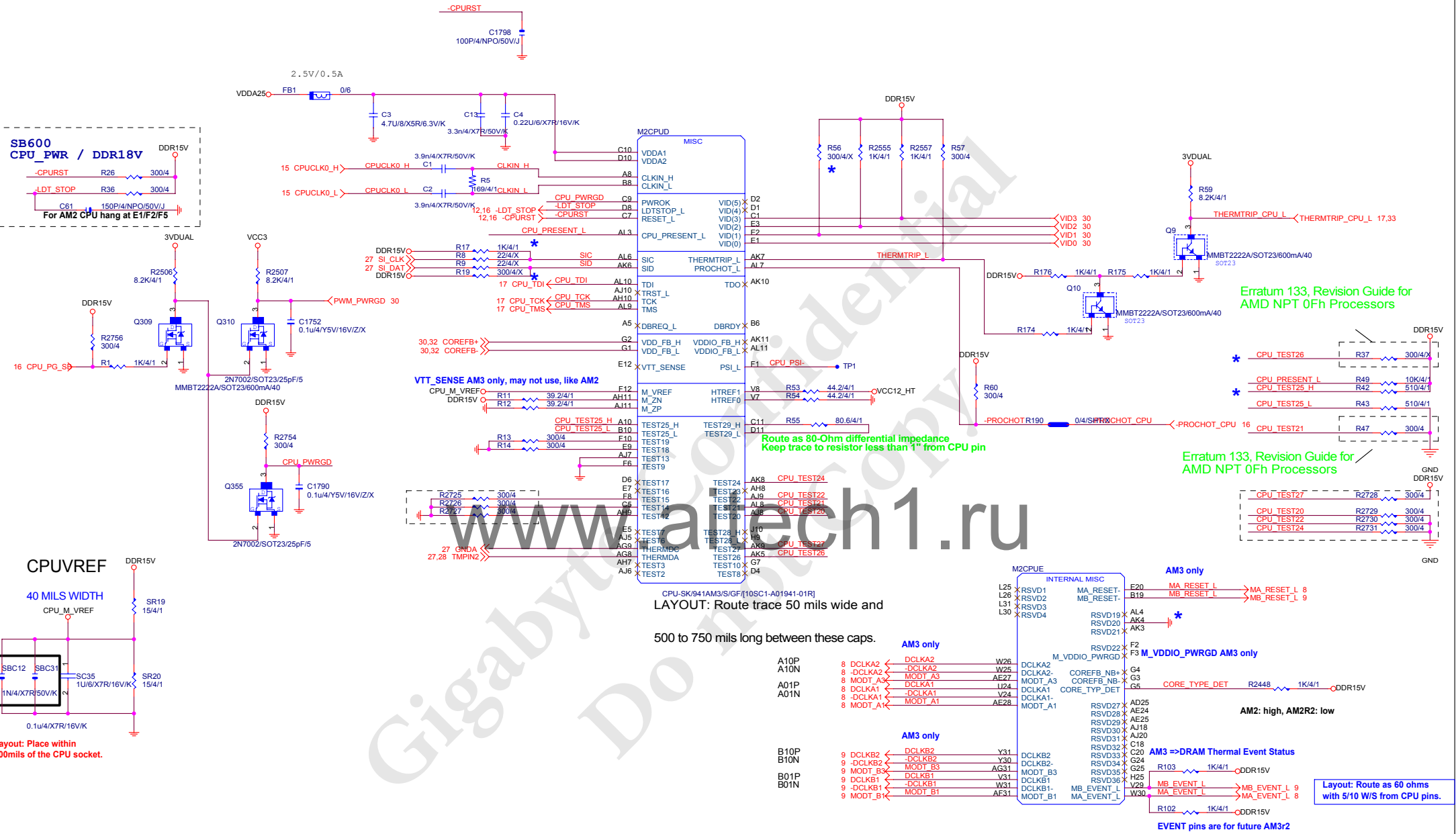
AM2RM/PP/BU/PB[12KRC-04K812-12R]



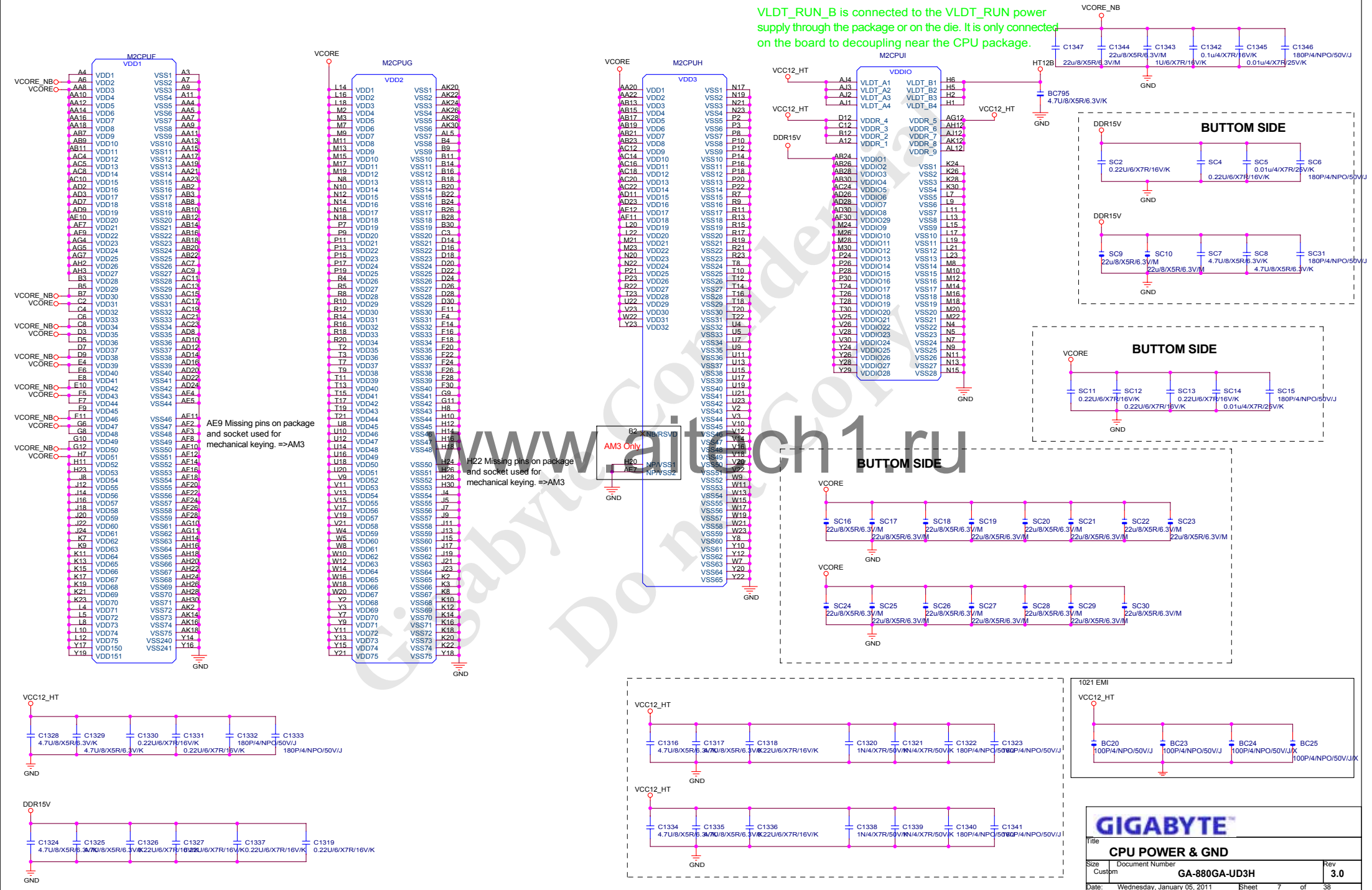
GIGABYTE			
Title CPU HYPER TRANSPORT			
Size Custom	Document Number GA-880GA-UD3H	Rev 3.0	
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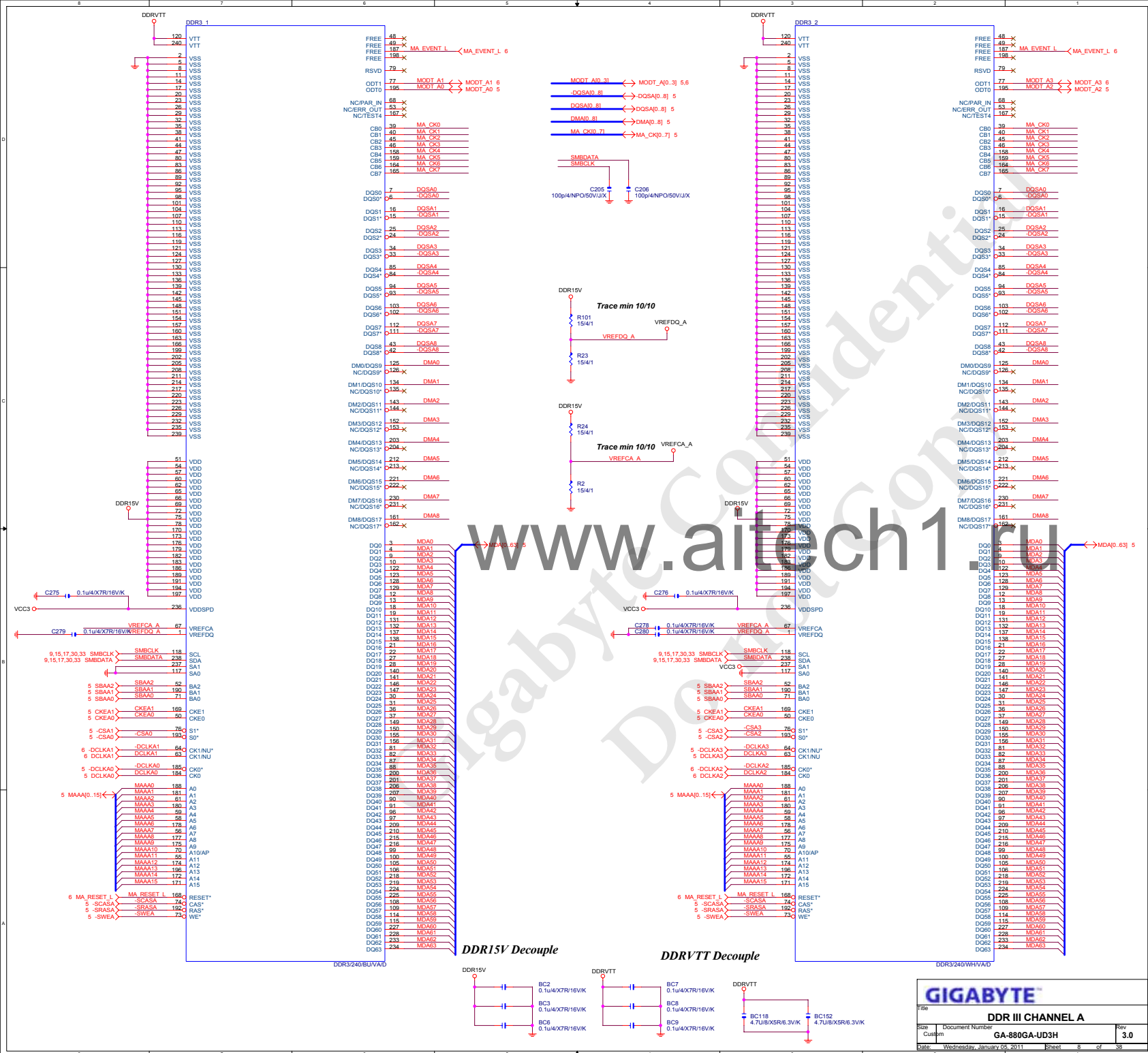


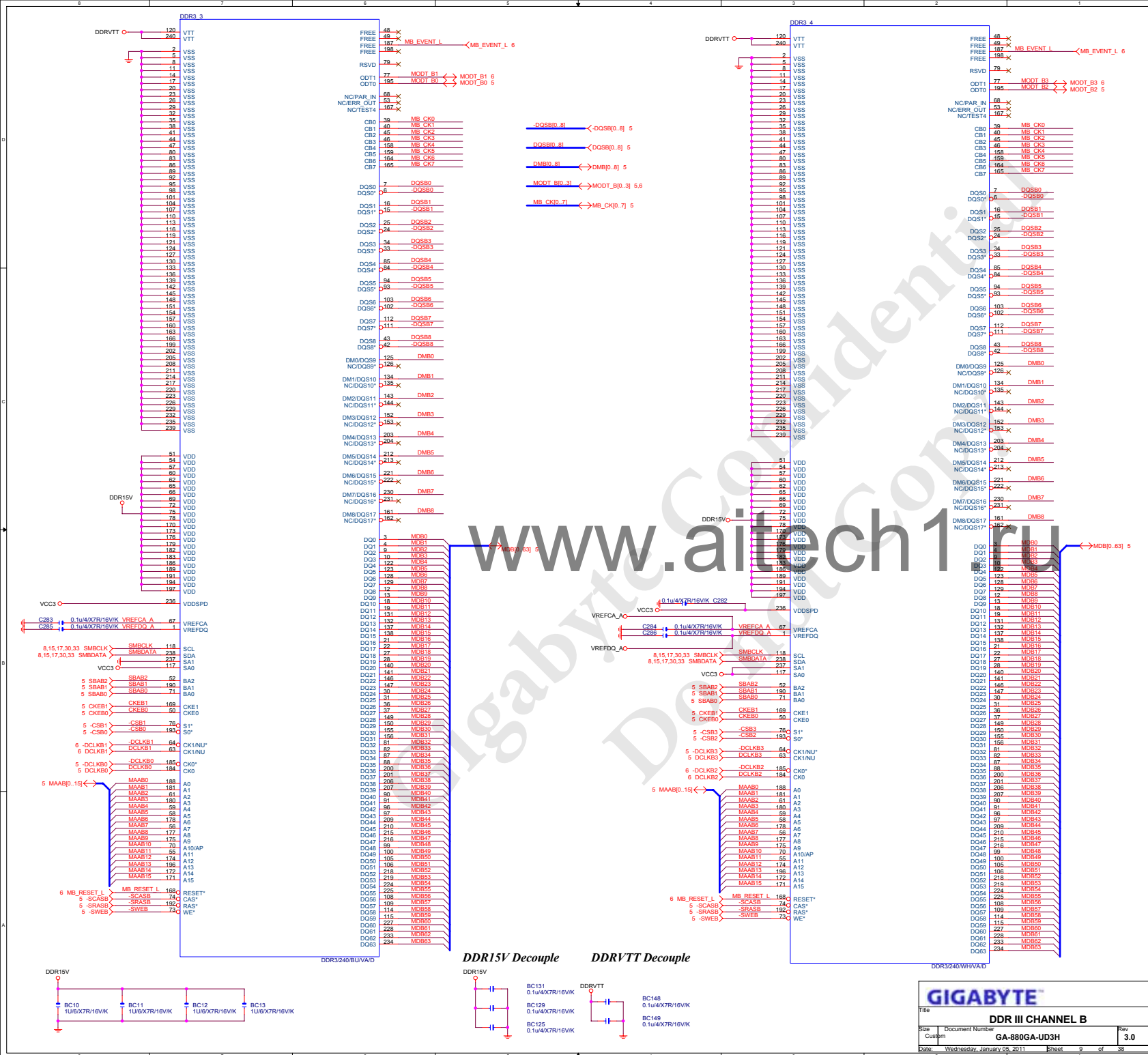
GIGABYTE			
CPU DDRIII MEMORY			
Title	CPU DDRIII MEMORY		
Size	Document Number	Rev	
Custom	GA-880GA-UD3H	3.0	
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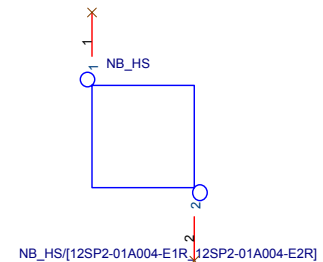


VLDT_RUN_B is connected to the VLDT_RUN power supply through the package or on the die. It is only connected on the board to decoupling near the CPU package.

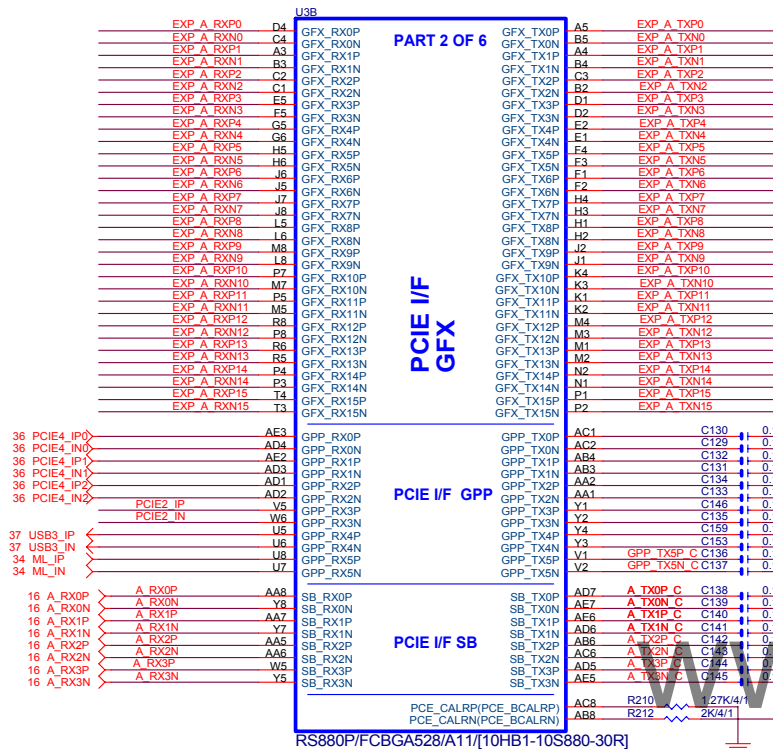






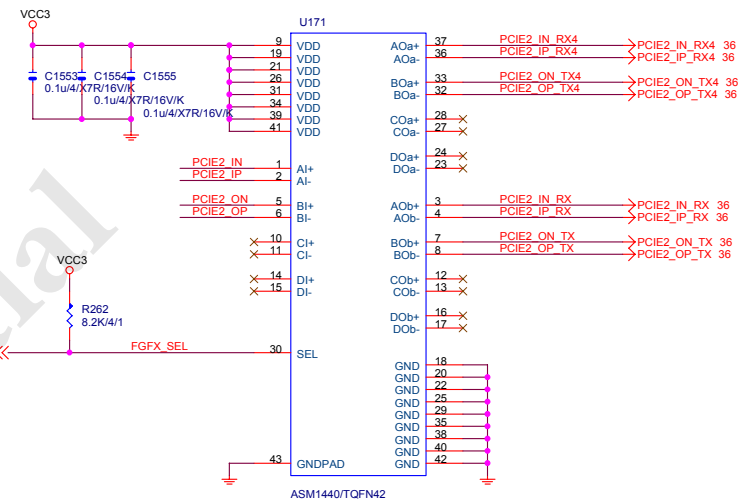


EXP A_RXP0_15] >> EXP_A_RXP0_15] 20 EXP A_TXP0_15] >> EXP_A_TXP0_15] 20
EXP A_RXN0_15] >> EXP_A_RXN0_15] 20 EXP A_TXN0_15] >> EXP_A_TXN0_15] 20



Function	SEL
xI--> xOa	L (X4)
xI--> xOb	H (X1)

PLACE GAP CLOSE TO CONNECTOR



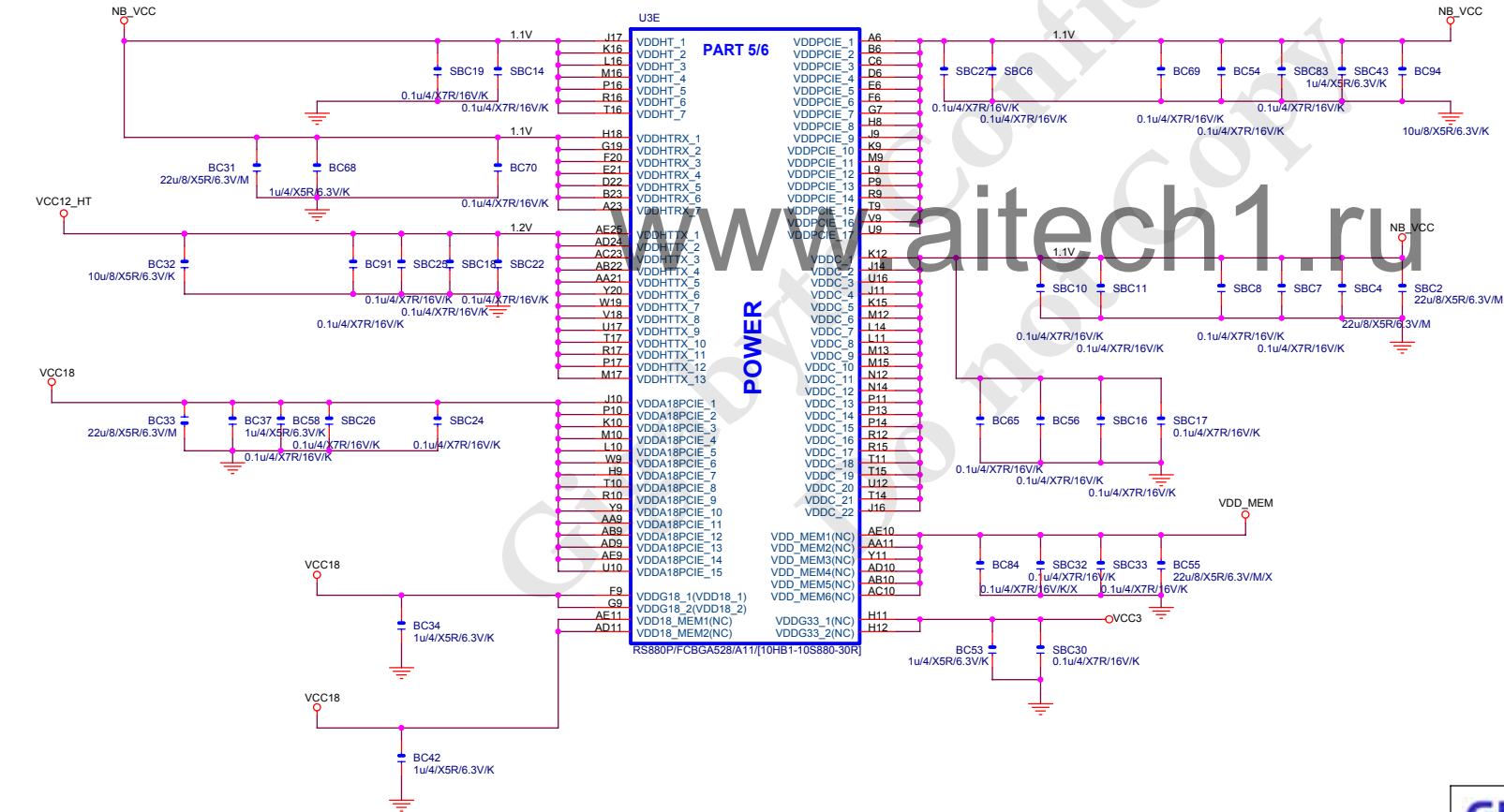
GIGABYTE®

Title RS880 PCIE I/F ,Switch

Size Document Number GA-880GA-UD3H Rev 3.0

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Please use 1mm pad size,
place all ELT test pads
on bottom side only

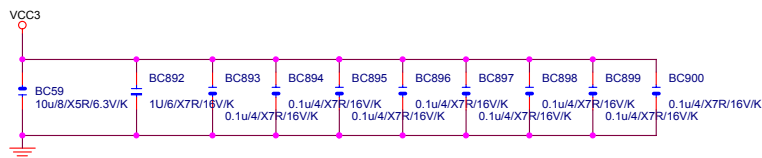


RS740/RX780/RS780 POWER DIFFERENCE TABLE

PIN NAME	RS740	RX780	RS780	PIN NAME	RS740	RX780	RS780
VDDHT	NC	+1.1V	+1.1V	IOPLLVD	+1.2V	NC	+1.1V
VDDHTRX	NC	+1.1V	+1.1V	AVDD	+3.3V	NC	+3.3V
VDDHTTX	+1.2V	+1.2V	+1.2V	AVDDDI	+1.8V	NC	+1.8V
VDDA18PCIE	NC	+1.8V	+1.8V	AVDDQ	+1.8V	NC	+1.8V
VDD18	+1.8V	+1.8V	+1.8V	PLLVD	+1.2V	NC	+1.1V
VDD18_MEM	NC	NC	+1.8V	PLLVD18	+1.8V	NC	+1.8V
VDDPCIE	+1.2V	+1.1V	+1.1V	VDDA18PCIEPLL	+1.2V	+1.8V	+1.8V
VDDC	+1.2V	+1.1V	+1.1V	VDDA18HTPLL	+1.8V	+1.8V	+1.8V
VDD_MEM	+1.8V	NC	+1.8V(DDR2) +1.5V(DDR3)	VDDLTP18	+1.8V	NC	+1.8V
VDD33	+3.3V	NC	+3.3V	VDDL18	+1.8V	NC	+1.8V
IOPLLVD18	+1.8V	NC	+1.8V	VDDL33	+3.3V	NC	NC

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Title			RS880 POWER & GND	
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- 1- PLACE ALL THE SERIES TERMINATION RESISTORS AS CLOSE TO U800 AS POSSIBLE
- 2- ROUTE ALL SRCCLKTx AND SRCCLKCx AS DIFFERENT PAIR RULE
- 3- PUT DECOUPLING CAPS CLOSE TO U800 POWER PIN

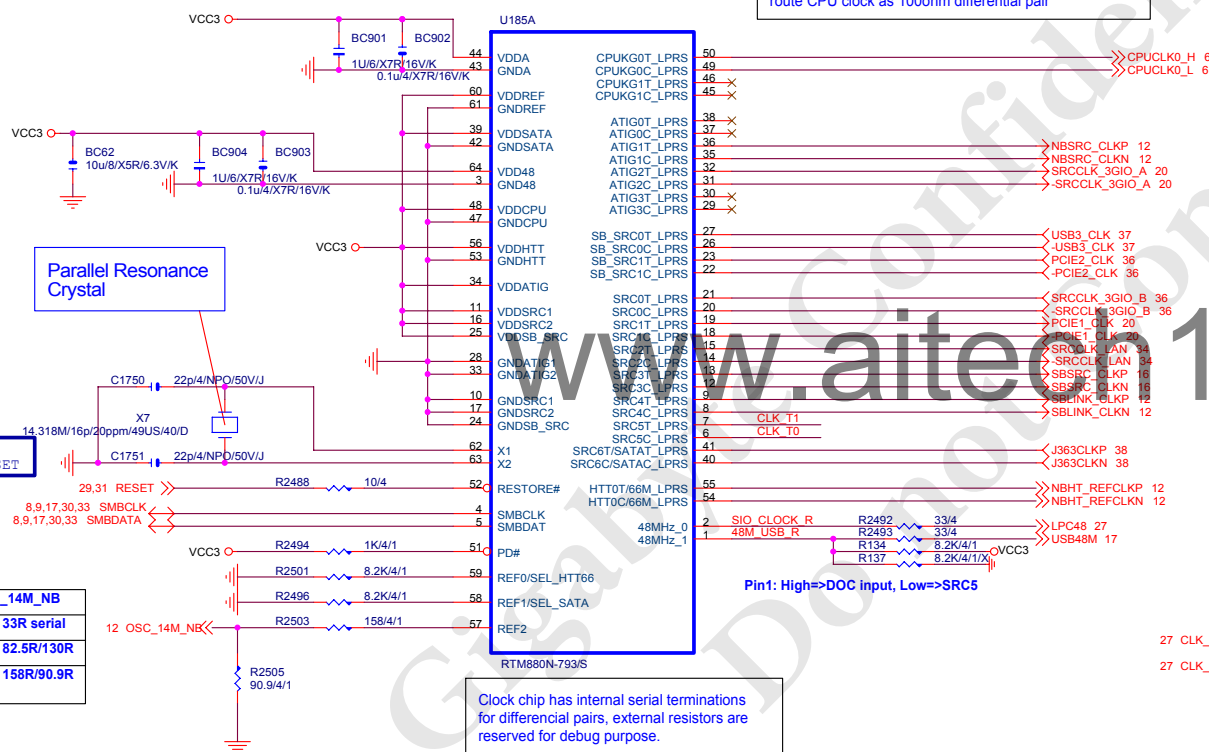


Place R800/801 less than 500 mils away from U800
R851 less than 100 mils away from R800/801
route CPU clock as 100ohm differential pair

NB CLOCK INPUT TABLE

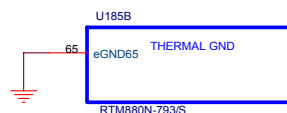
NB CLOCKS	RS740	RX780	RS780	
HT_REFCLKP	66M SE(SE)	100M DIFF	100M DIFF	
HT_REFCLKN	NC	100M DIFF	100M DIFF	
REFCLK_P	14M SE (3.3V)	14M SE (1.8V)	14M SE (1.1V)	100M DIFF
REFCLK_N	NC	NC	vref	100M DIFF
GFX_REFCLK*	100M DIFF	100M DIFF	100M DIFF	
GPP_REFCLK	NC	100M DIFF	100M DIFF(OUT)	
GPPSB_REFCLK	100M DIFF	100M DIFF	100M DIFF	

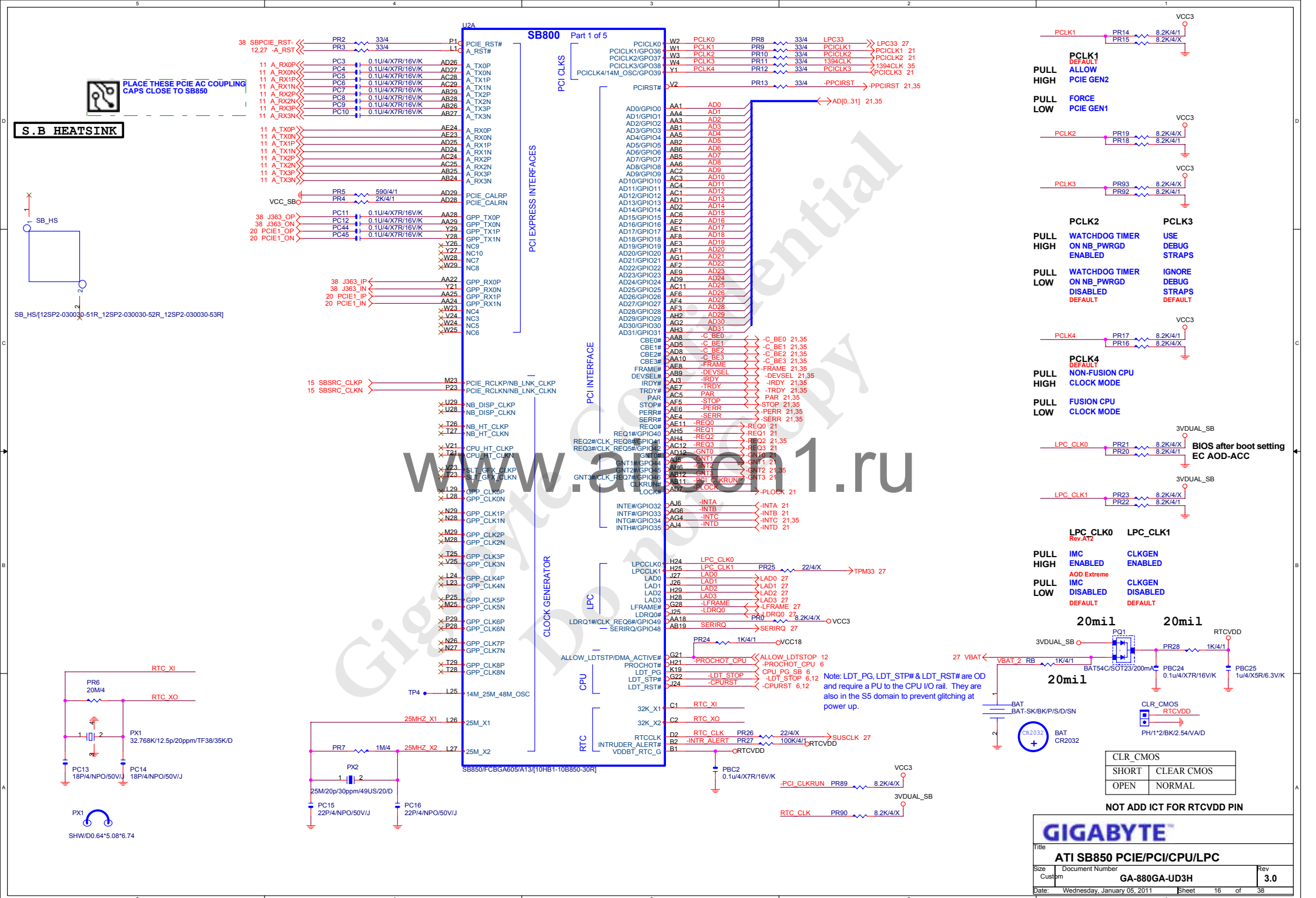
* the GFX_REFCLK input is required for all cases

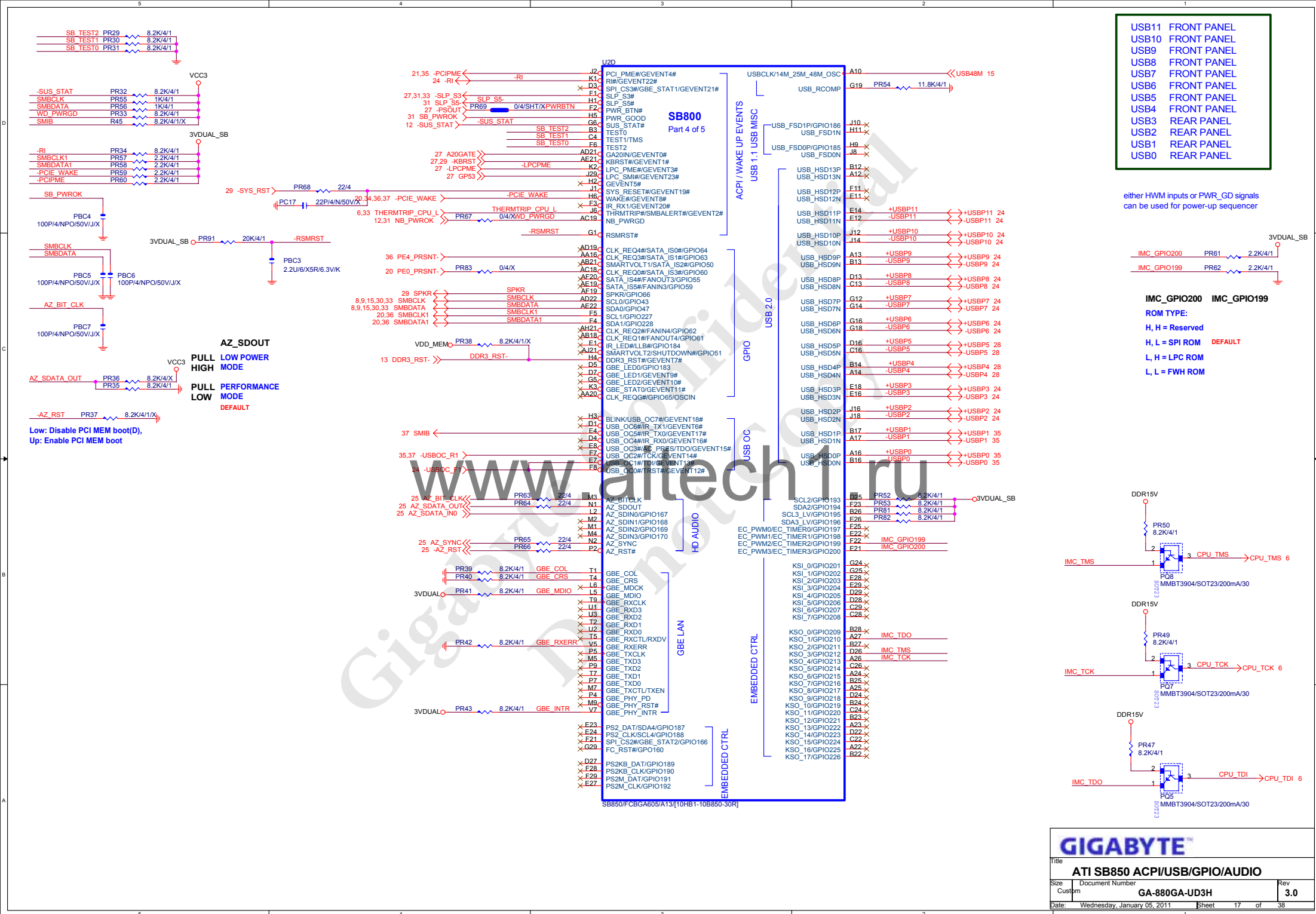


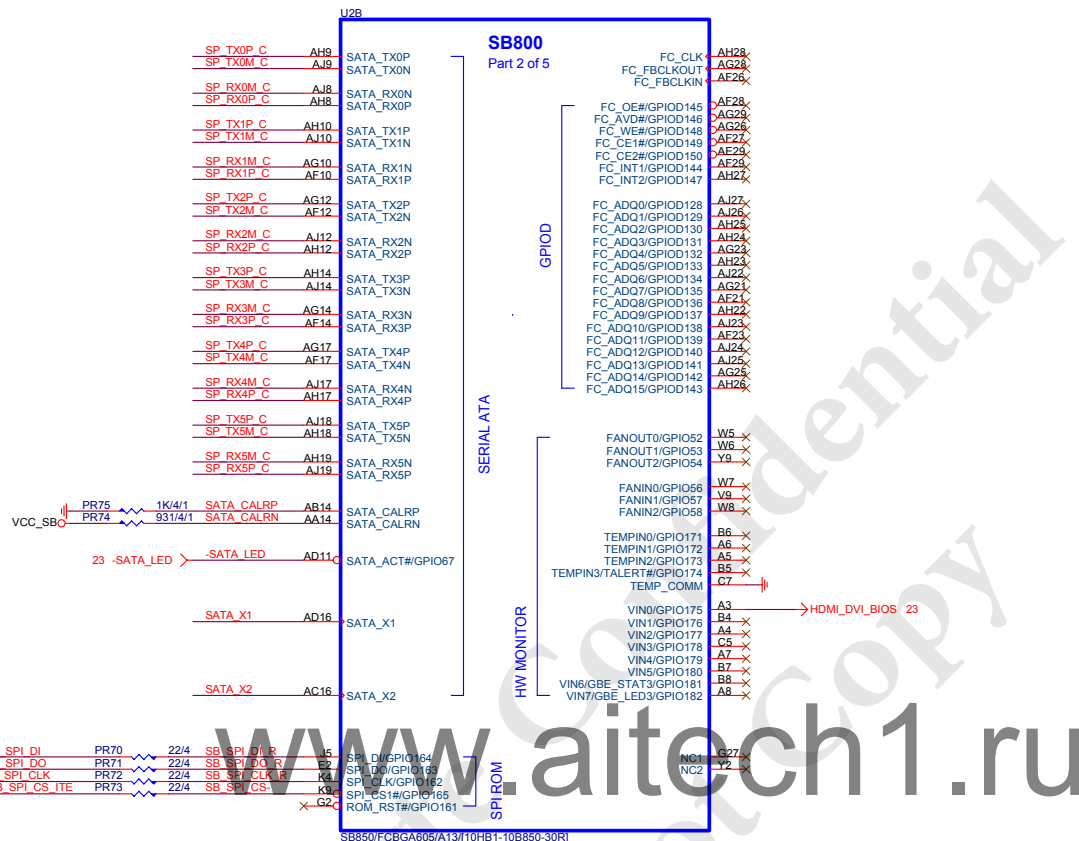
REF0/SEL_HTT66	HTT CLOCK
0	100.00 DIFFERENTIAL
1	66.66 SINGLE END

REF1/SEL_SATA	SRC6/SATA
0	100.00 DIFFERENTIAL SPREADING SRC CLOCK
1	100.00 NON-SPREADING DIFFERENTIAL SATA CLOCK





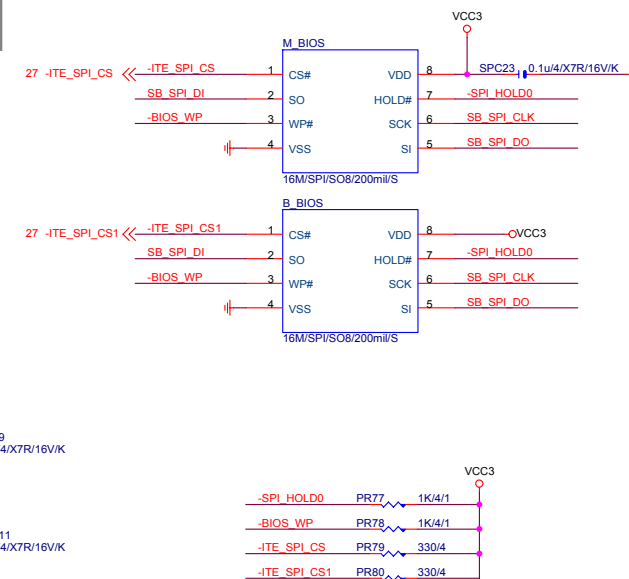
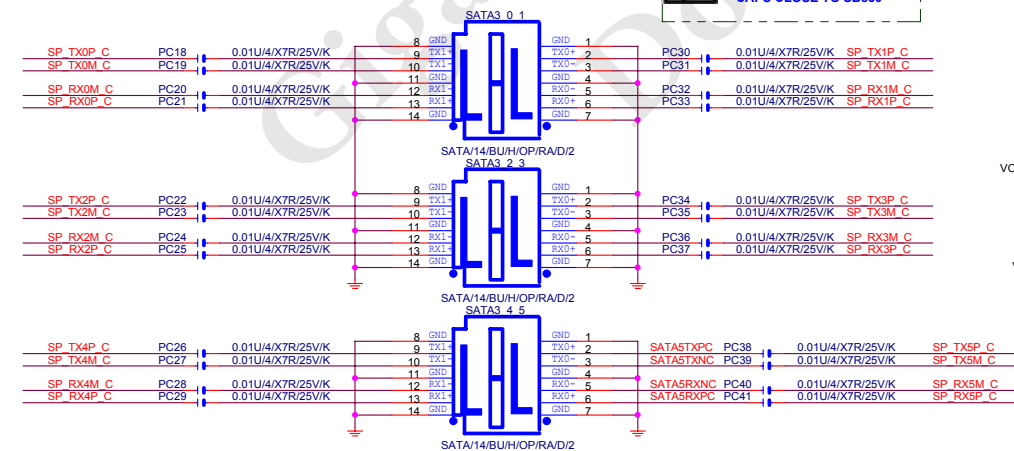




PLACE SATA_CAL
RES VERY CLOSE
TO BALL OF U600

NOTE :

**R650 IS 1K 1% FOR 25MHz
XTAL, 4.99K 1% FOR 100MHz
INTERNAL CLOCK**



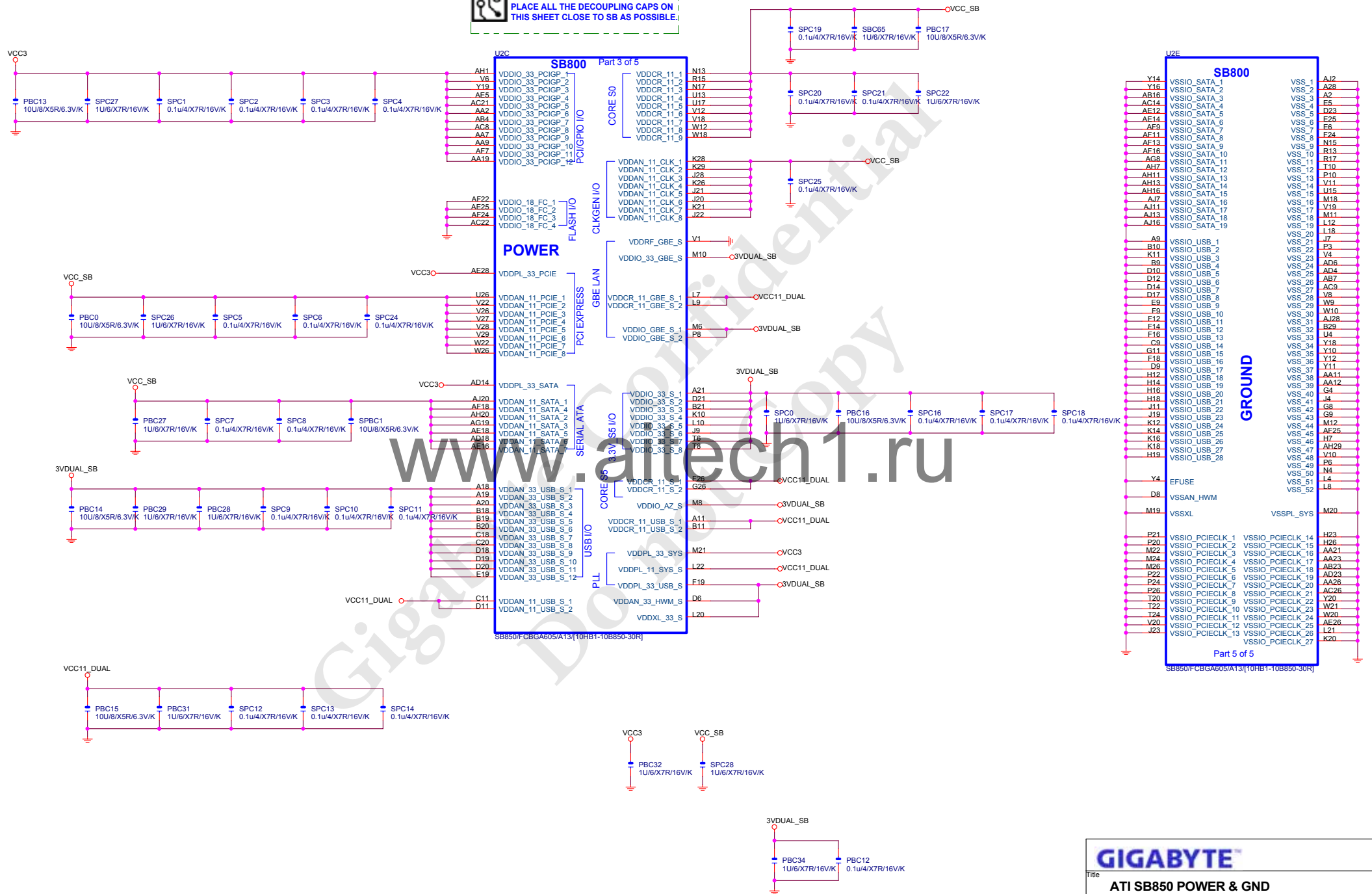
GIGABYTE™

Title	ATI SB850 SATA/IDE/HWM/SPI
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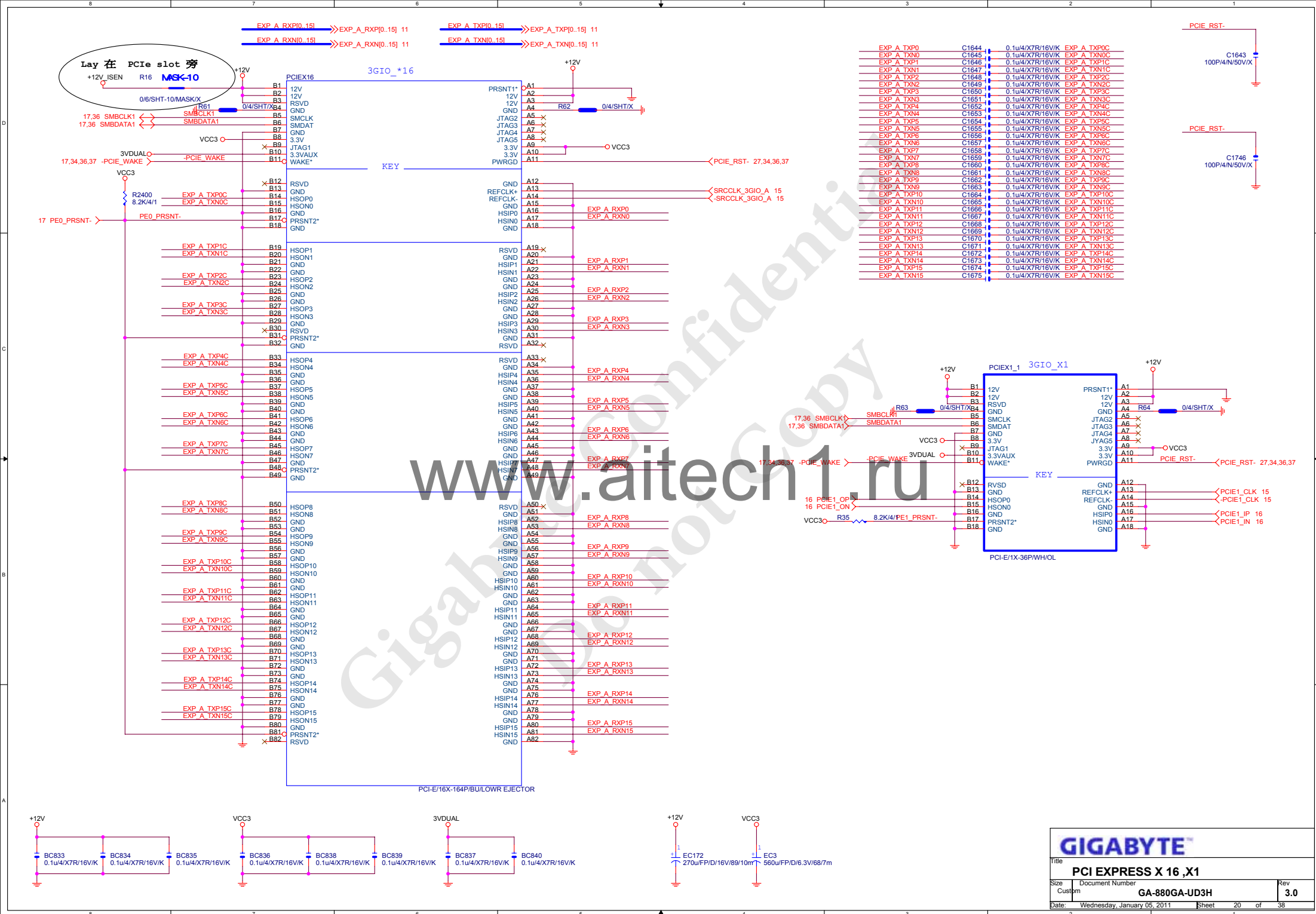
PLACE ALL THE DECOUPLING CAPS ON THIS SHEET CLOSE TO SB AS POSSIBLE.

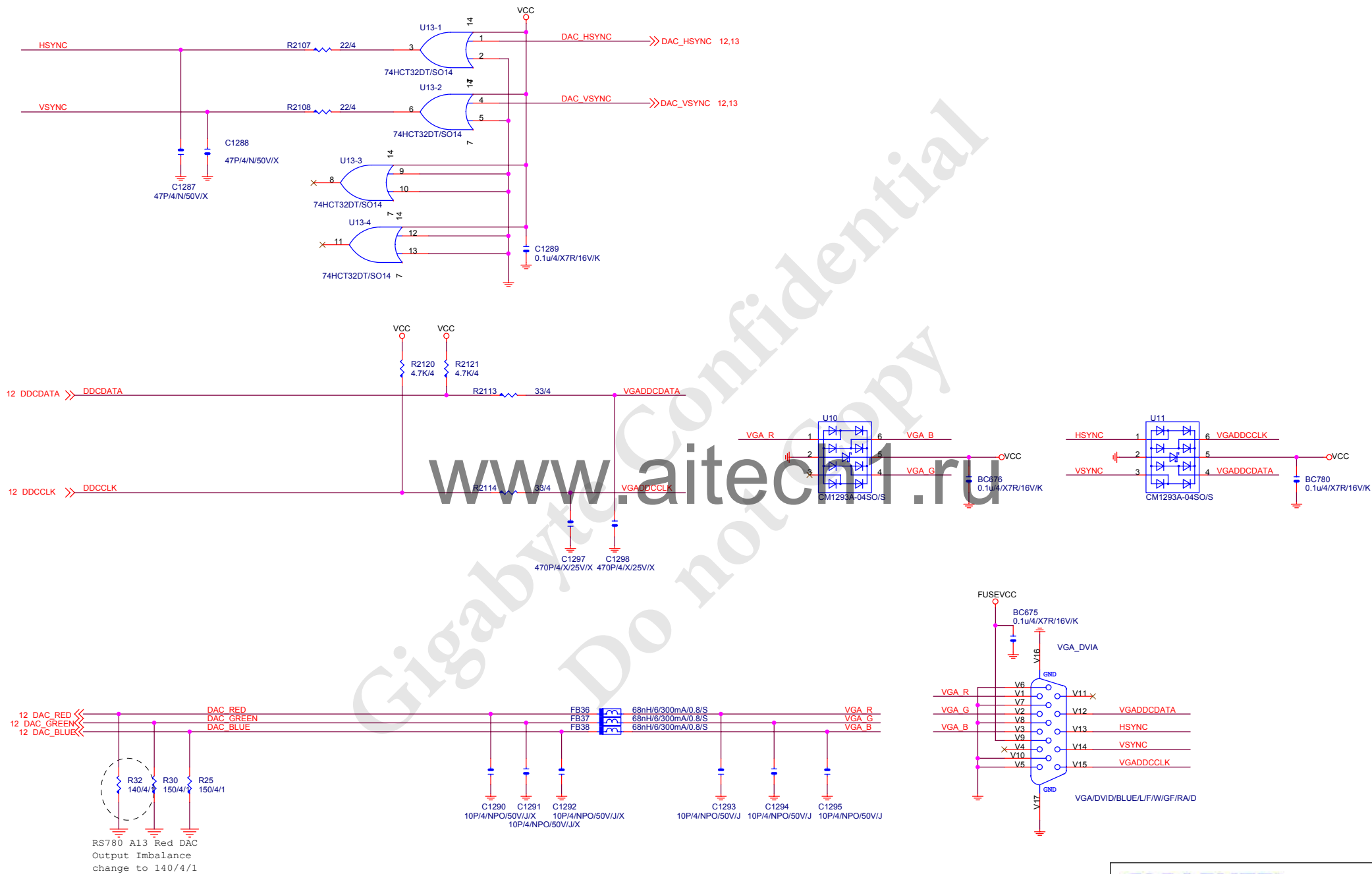


GIGABYTE

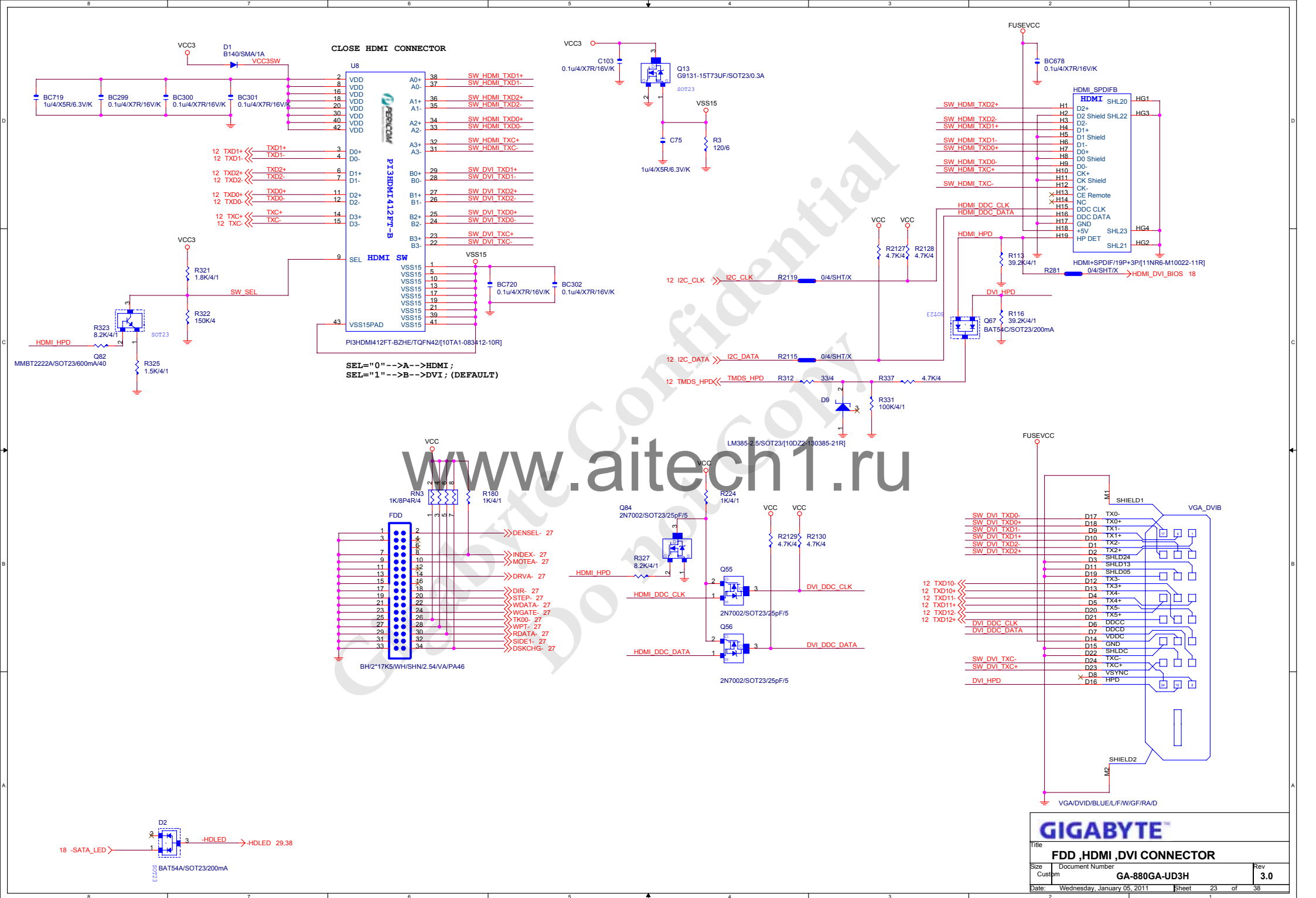
ATI SB850 POWER & GND

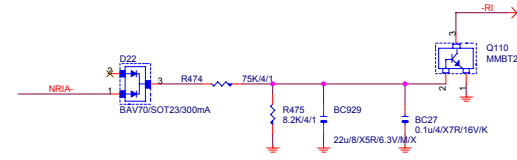
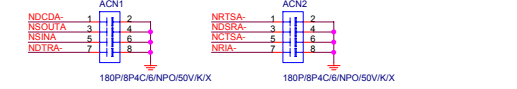
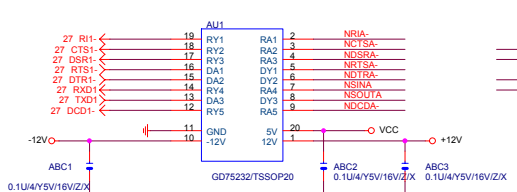
Size: Custom
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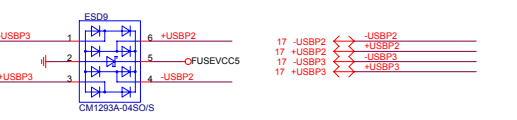
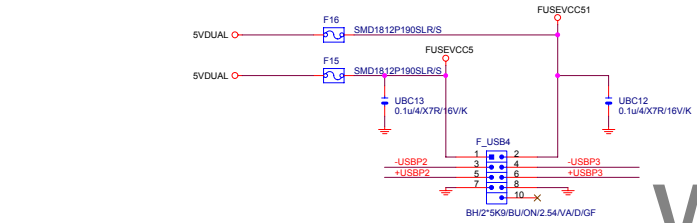


GIGABYTE™			
Title			
RGB			
Size	Document Number	Rev	
Custpm	GA-880GA-UD3H	3.0	
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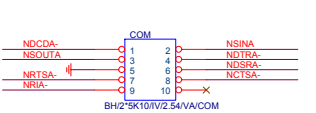
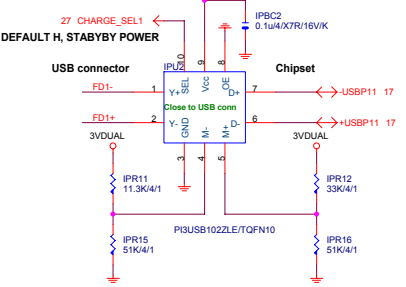
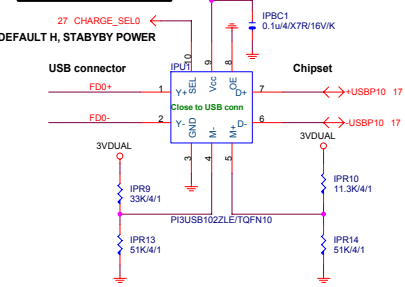




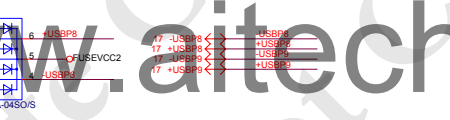
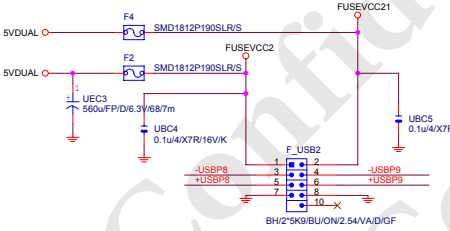
FRONT SIDE USB4



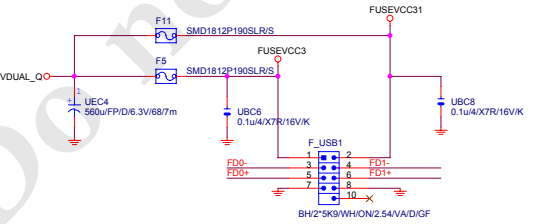
Phone charger circuit



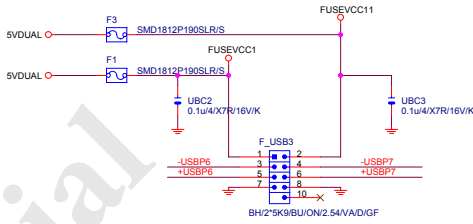
FRONT SIDE USB2



FRONT SIDE USB1



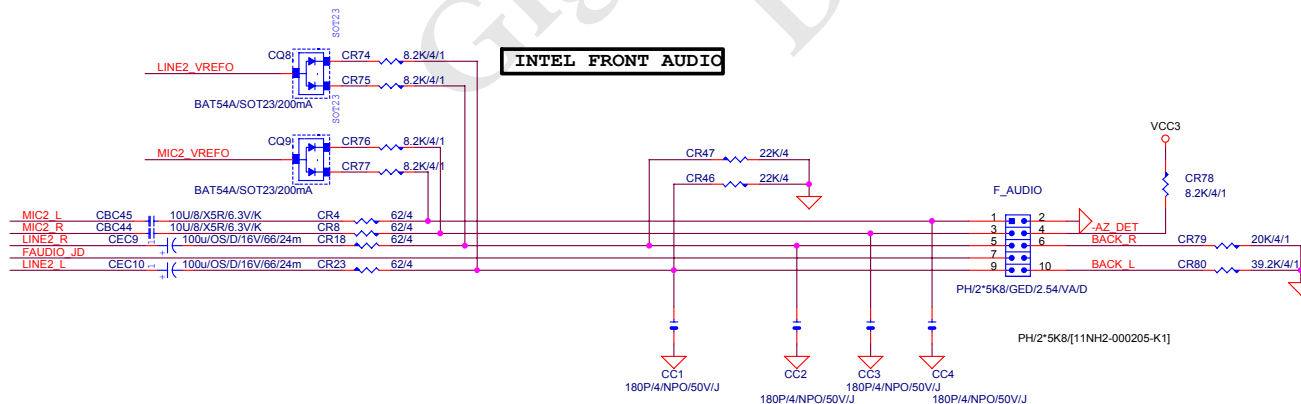
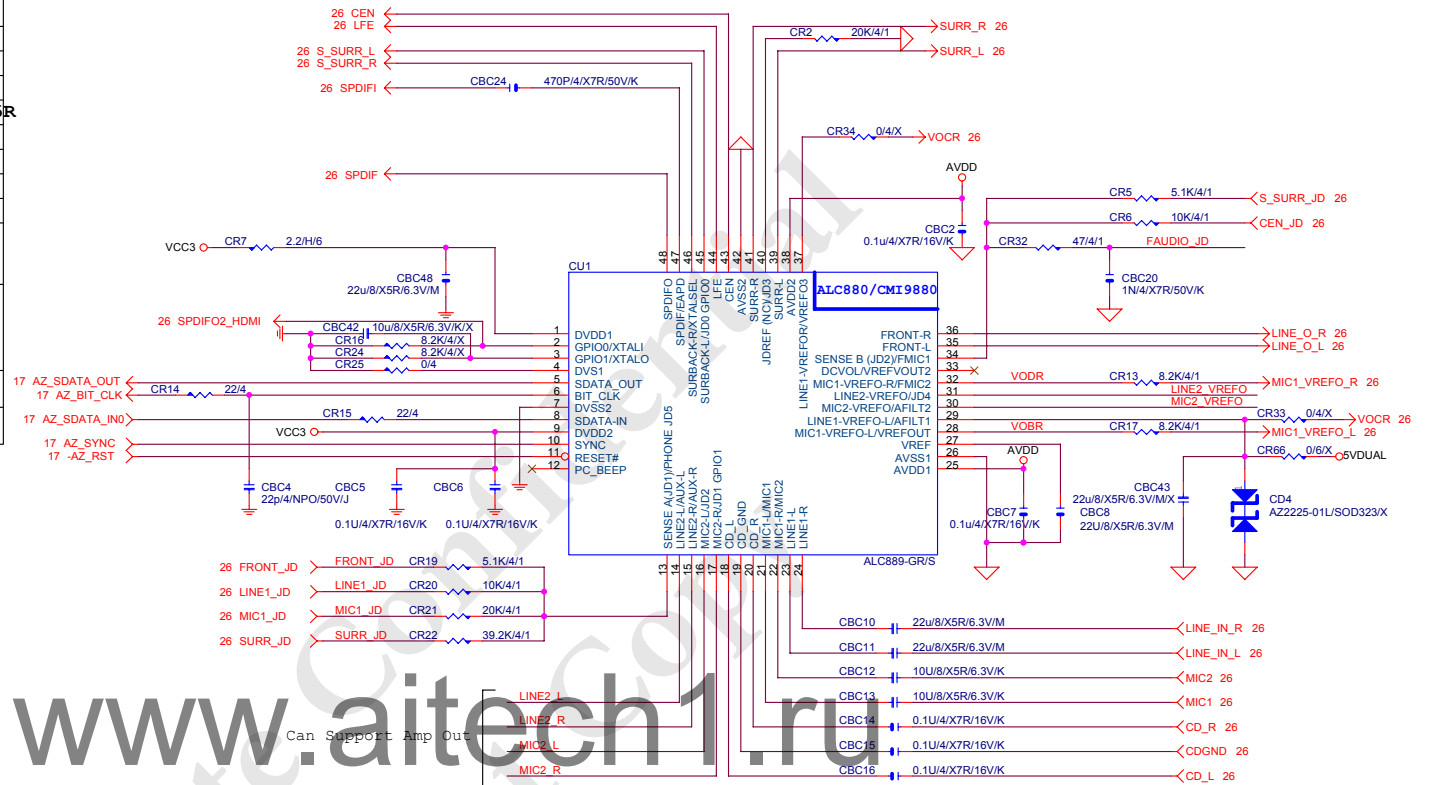
FRONT SIDE USB3

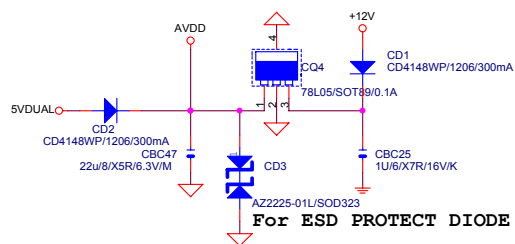
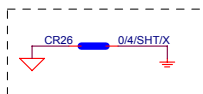


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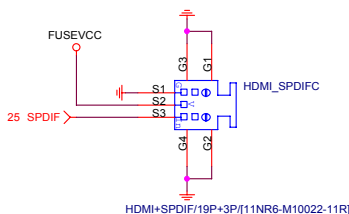
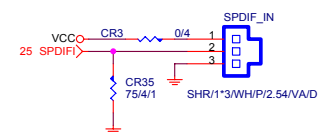
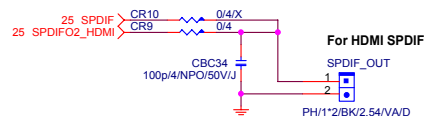
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	ALC892R	ALC889	ALC889A	ALC888	ALC892
CR16	X	X	O	X	X
CR24	X	X	O	X	X
CR25	X	O	O	O	X
CBC42	10uF/X5R	X	X	X	10uF/X5R
CR2	20K/1%	20K/1%	20K/0.1%	20K/1%	20K/1%
CR9	O	O	X	X	O
CR10	X	X	O	O	X
CBC10/CBC11/CBC12/ CBC13/CBC44/CBC45	4.7uF /X5R	10uF /X5R	4.7uF /X5R	4.7uF /X5R	4.7uF /X5R
CR4/CR8/CR18/CR23/ CR11/CR12/CR27/CR29/ CR49/CR50/CR43/CR44/ CR45/CR48/CR59/CR60	75 ohm or lower	66 ohm or lower	75 ohm	75 ohm	75 ohm
CR33/CD1/CD2/CD3/CQ4/ CBC25	O	O	O	O	X
CR34/CR66/CBC43/CD4	X	X	X	X	O

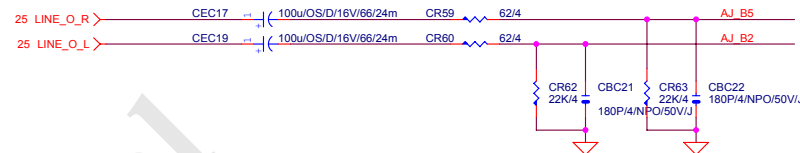




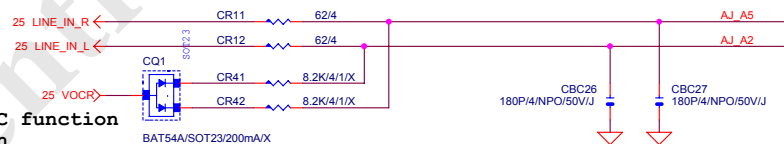
SPDIF



LINE OUT FRONT OUT

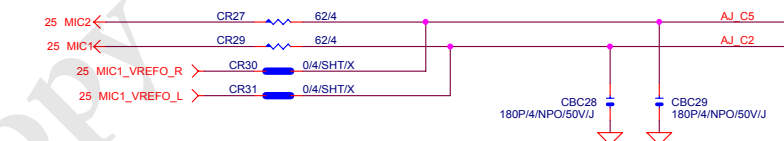


LINE-IN

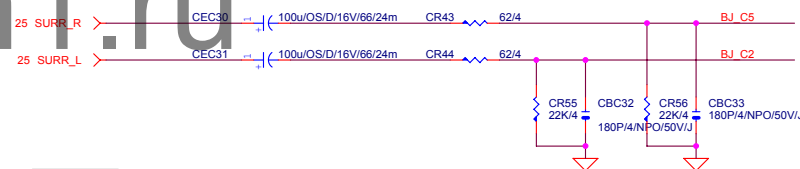


Verify MIC function
in LINE-in

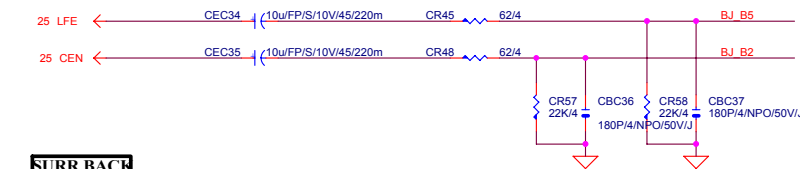
MIC



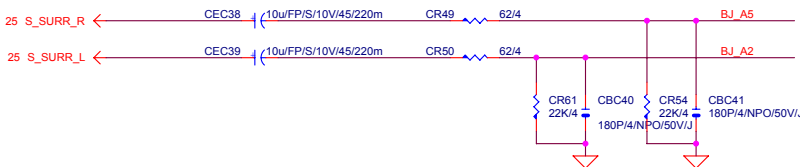
SURROUND



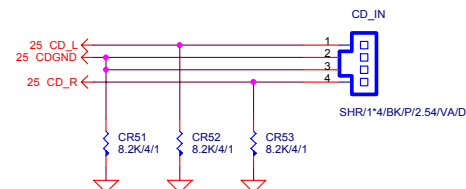
CEN/LFE



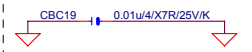
SURR BACK



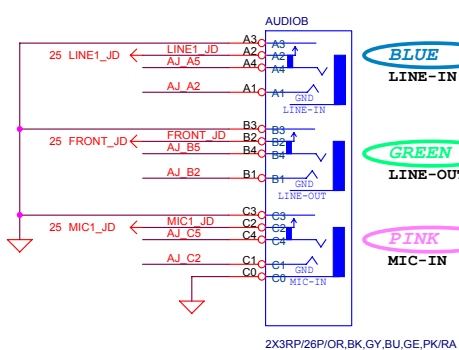
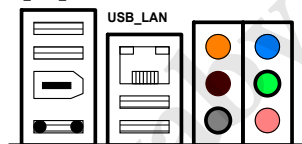
CD IN



For Audio precision test



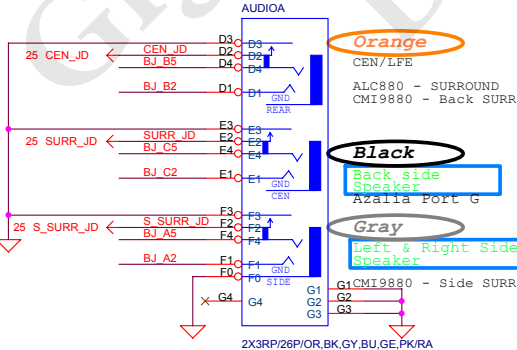
USB_1394_ESATA



BLUE
LINE-IN

GREEN
LINE-OUT

PINK
MIC-IN



Orange
CEN/LFE

Black
Back side
Speaker

Gray
Left & Right Side
Speaker

Gray
Left & Right Side
Speaker

Gray
Left & Right Side
Speaker

Gray
Left & Right Side
Speaker

A3R3/13P/B/[11NR6-403006-01_11NR6-403006-02]
3R3+15F/[11NR6-403004-11]

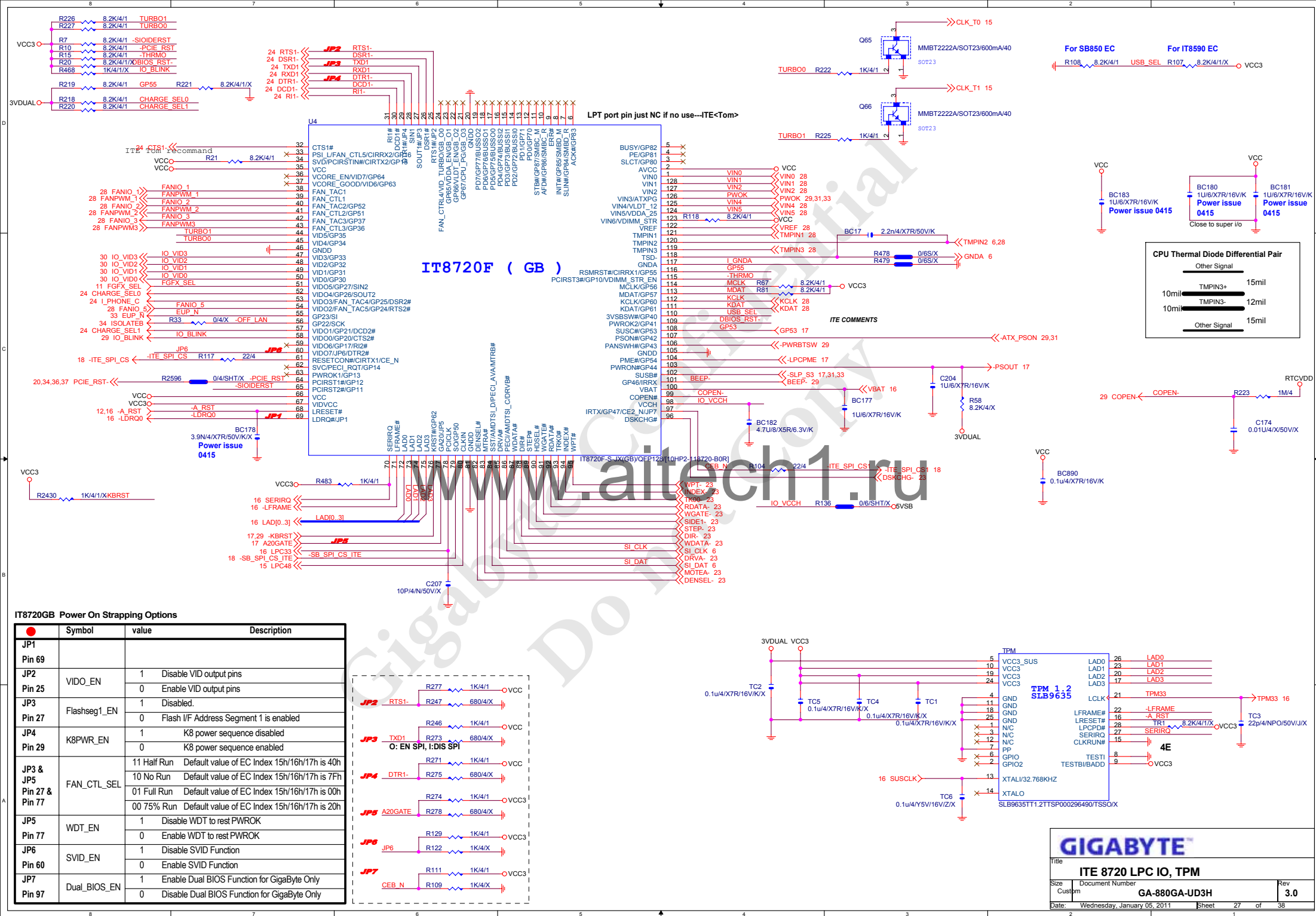
A3R3/13P/0BG/[11NR6-403006-71]
3R3+15F/[11NR6-403004-31]

GIGABYTE

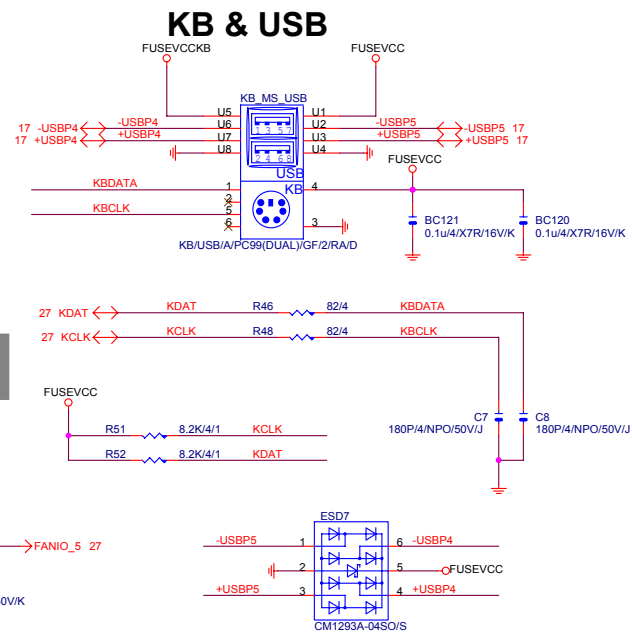
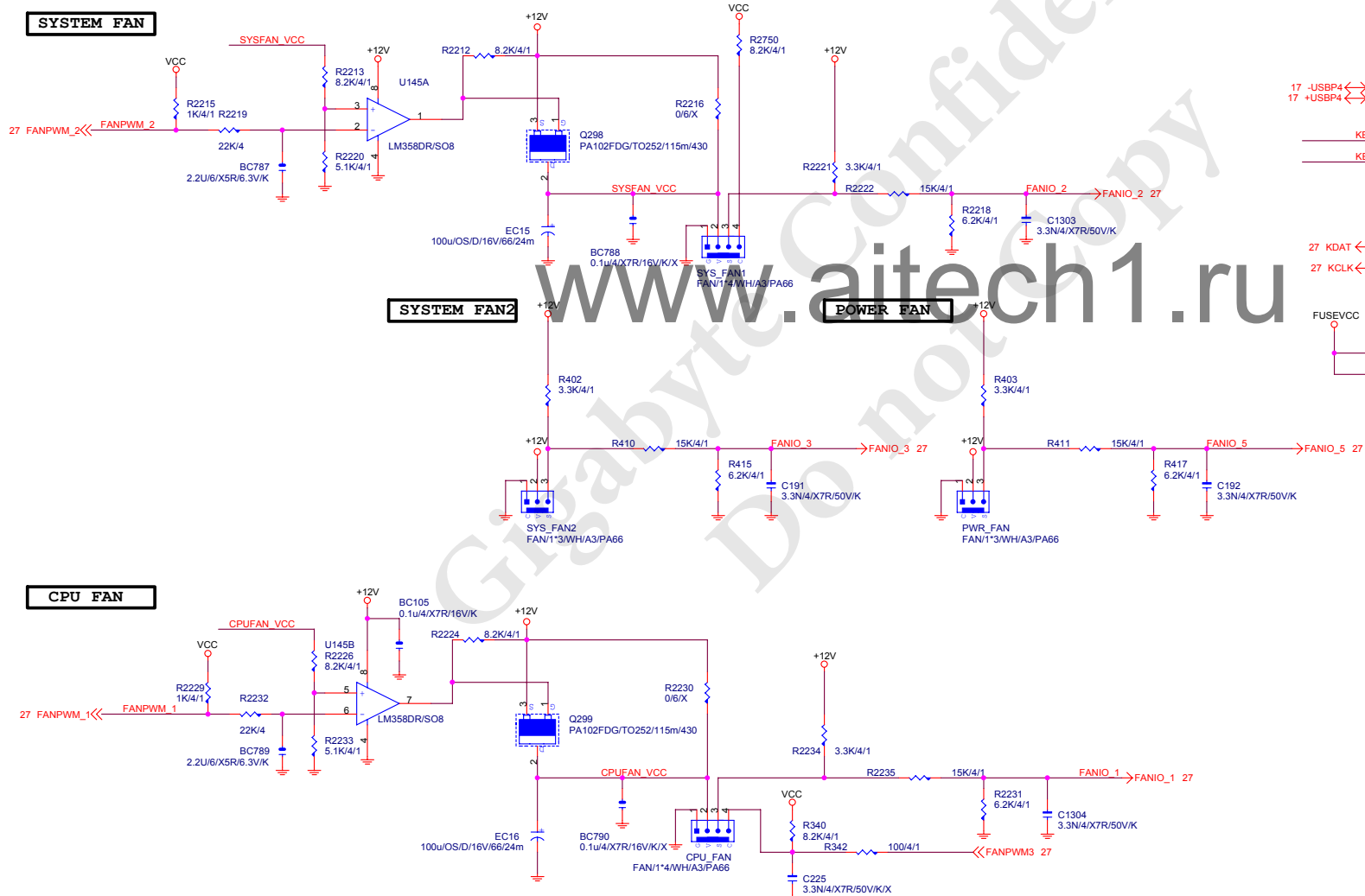
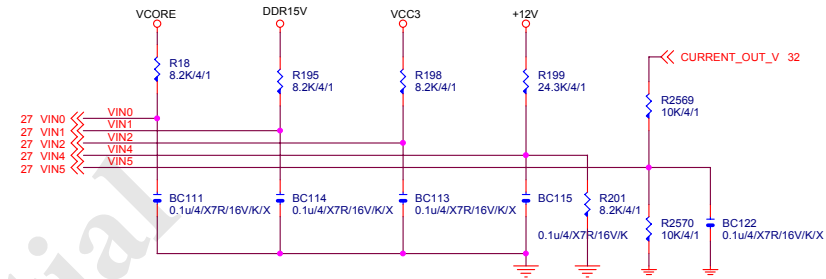
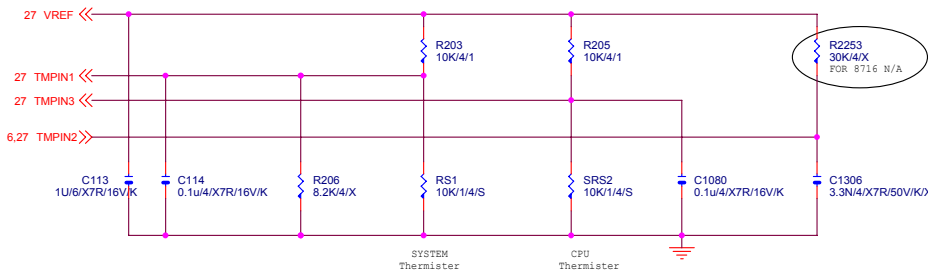
Title
AUDIO JACK

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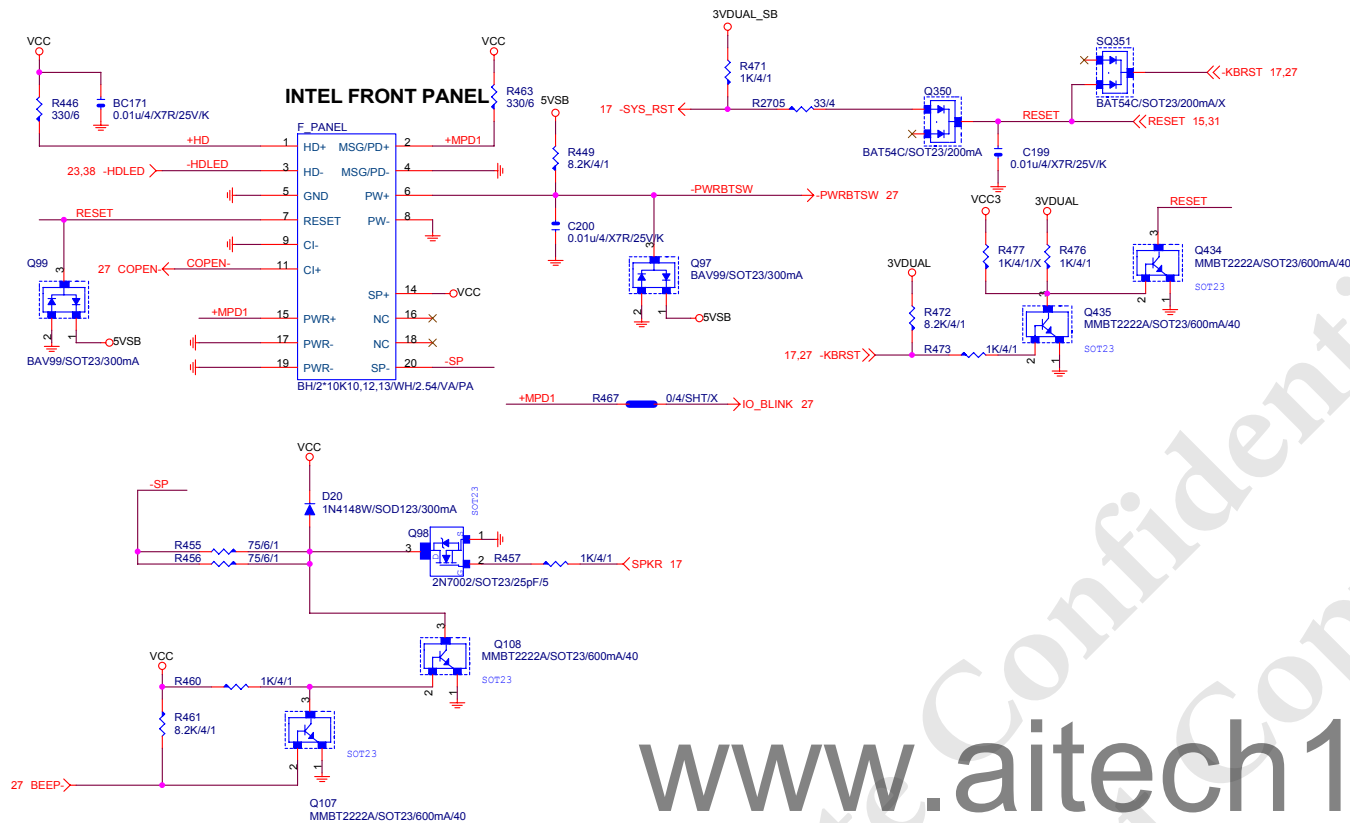


Hardware Monitor circuits

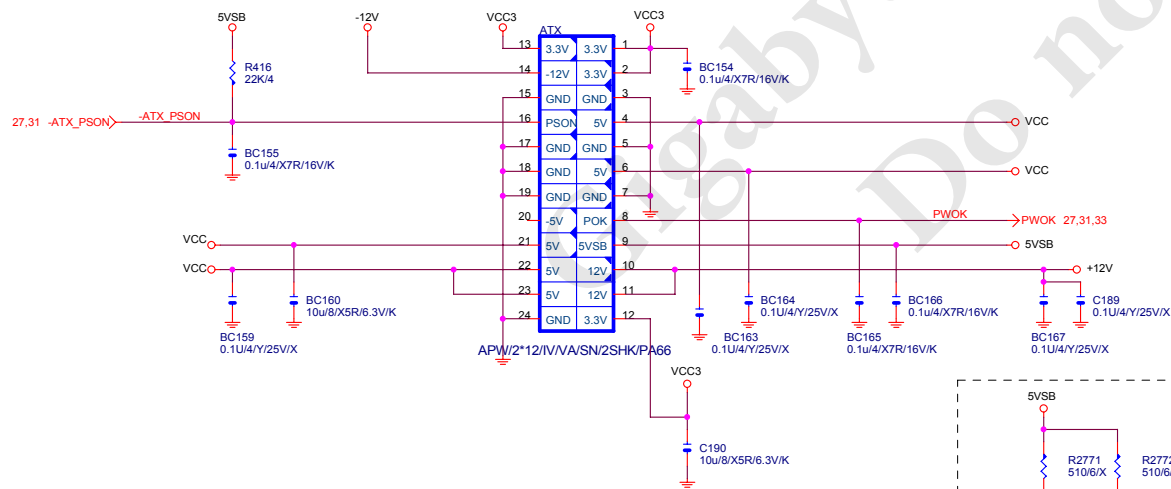


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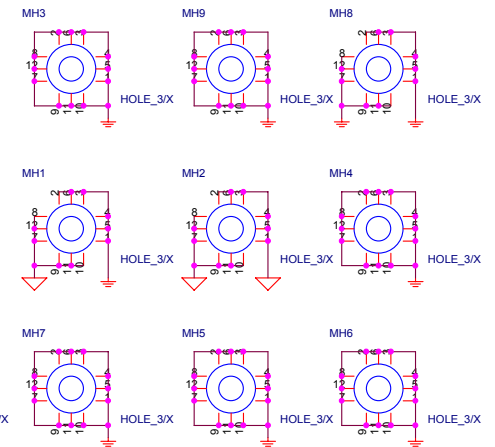
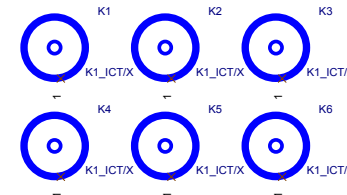
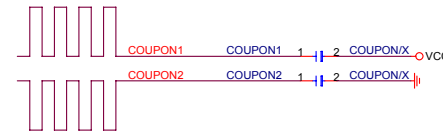
INTEL FRONT PANEL



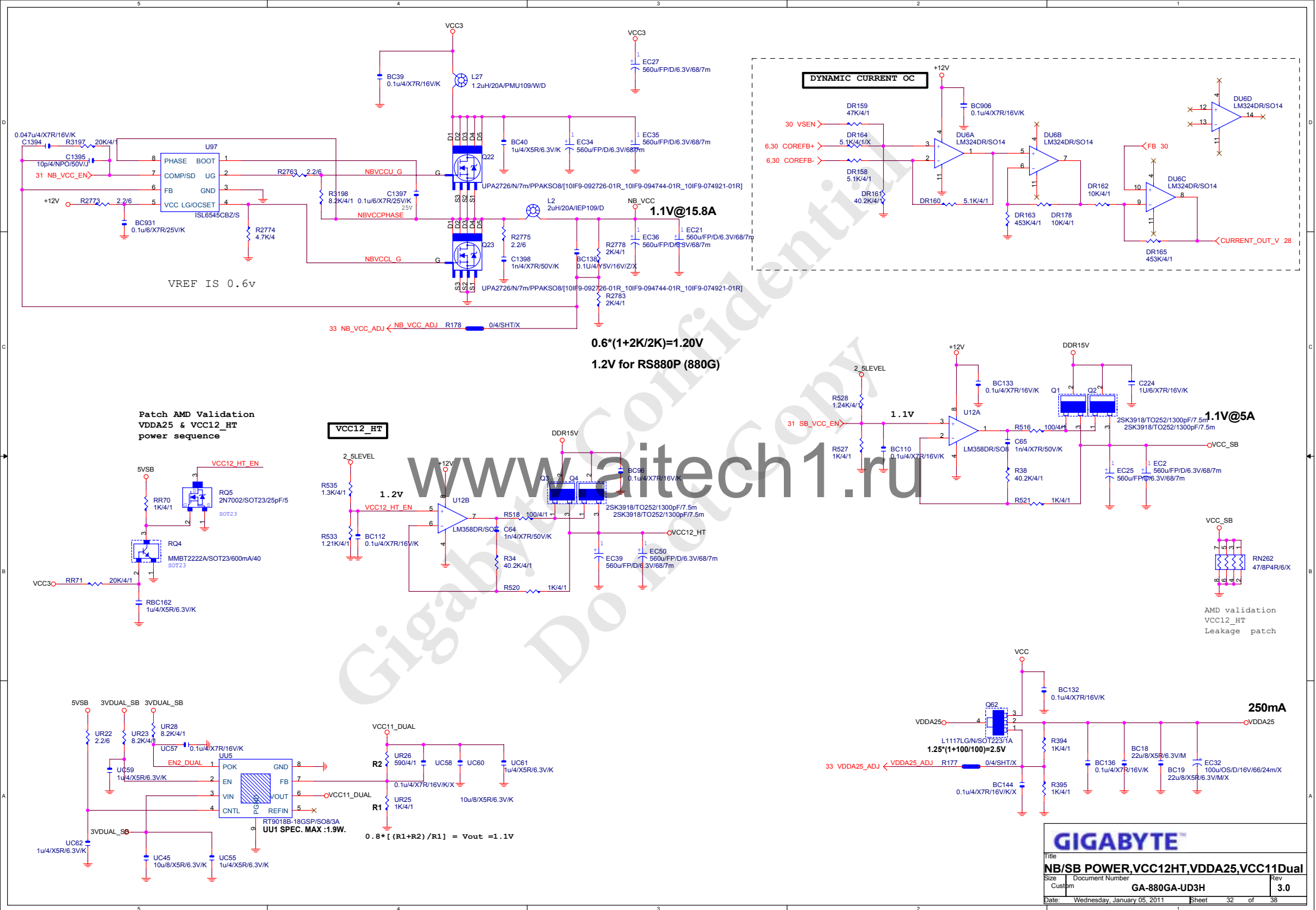
ATX POWER CONNECTOR

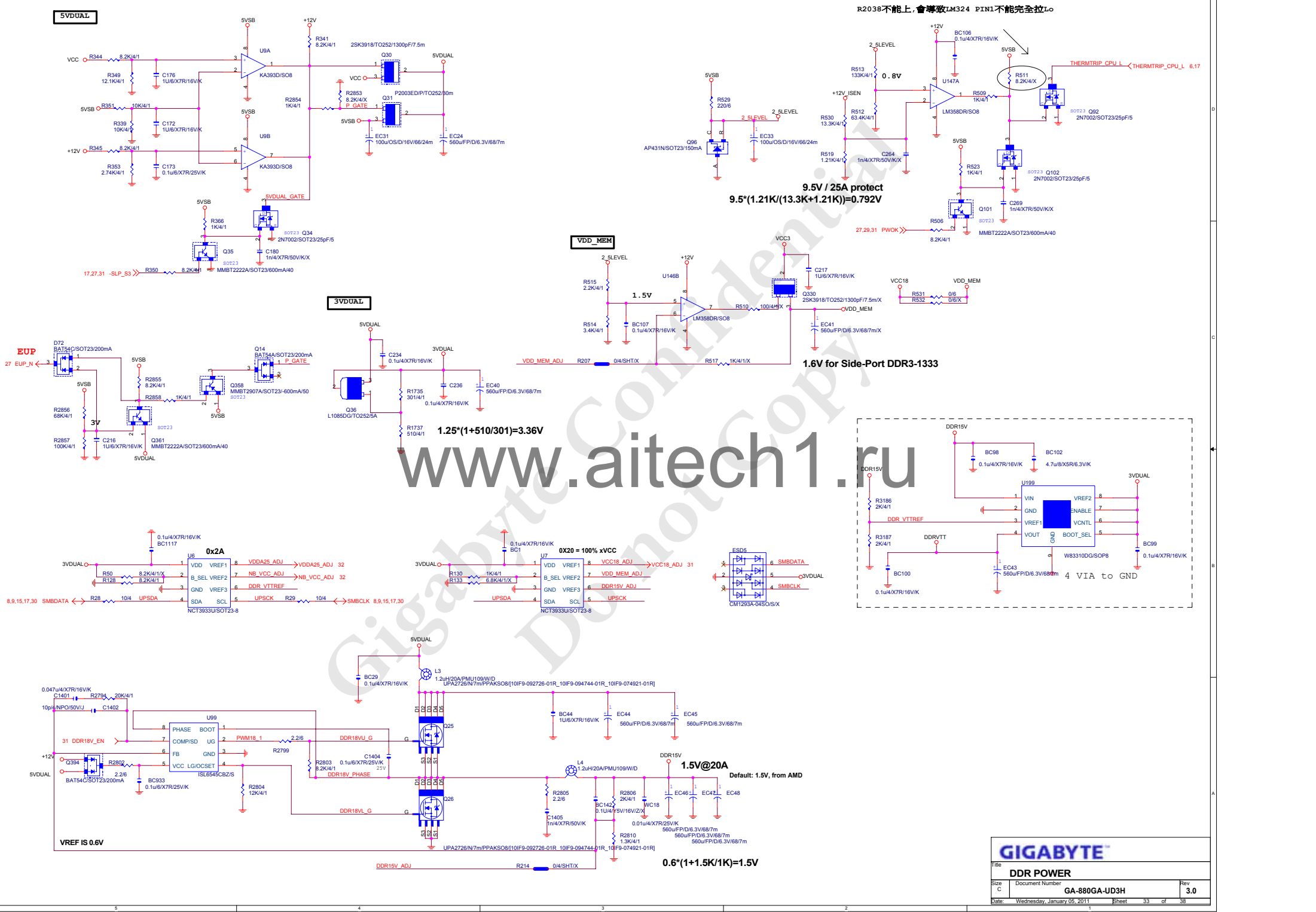


For Seasonic 900W
Power supply
cant Boot issue



GIGABYTE™			
Title ATX, FRONT PANEL ,EC			
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R2038不能上, 會導致LM324 PIN1不能完全拉Lo

9.5V / 25A protect
 $9.5 \times (1.21K / (13.3K + 1.21K)) = 0.792V$

1.6V for Side-Port DDR3-1333

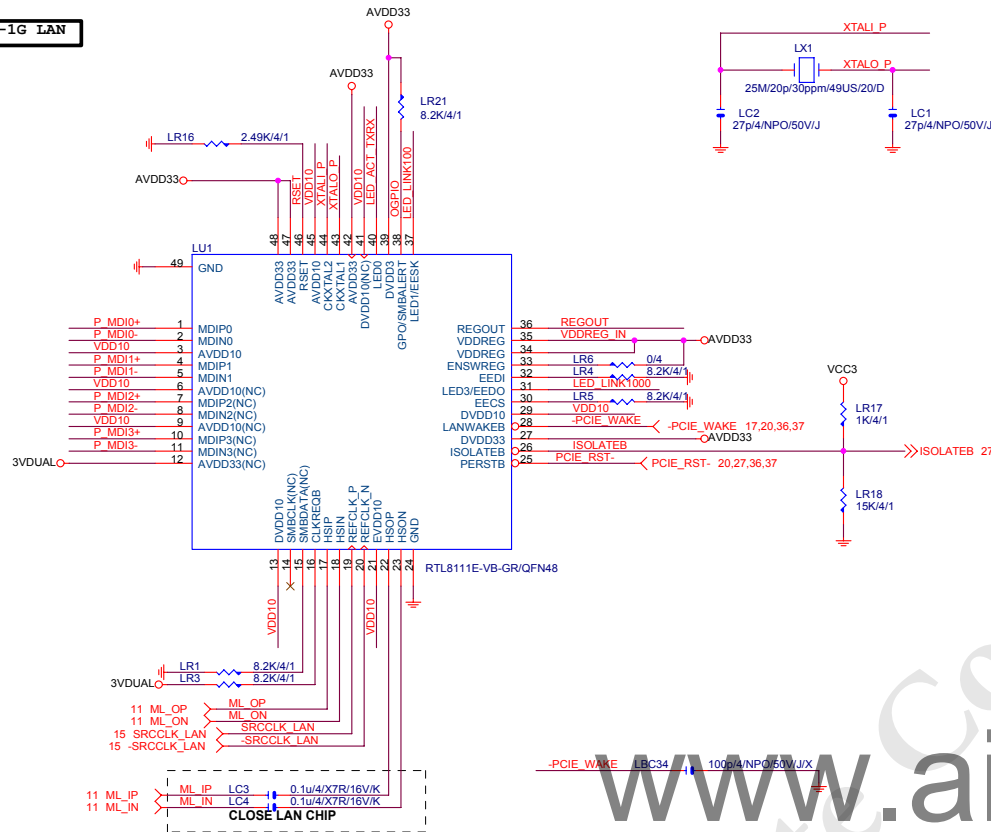
www.aitech1.ru

1.5V@20A
Default: 1.5V, from AMD

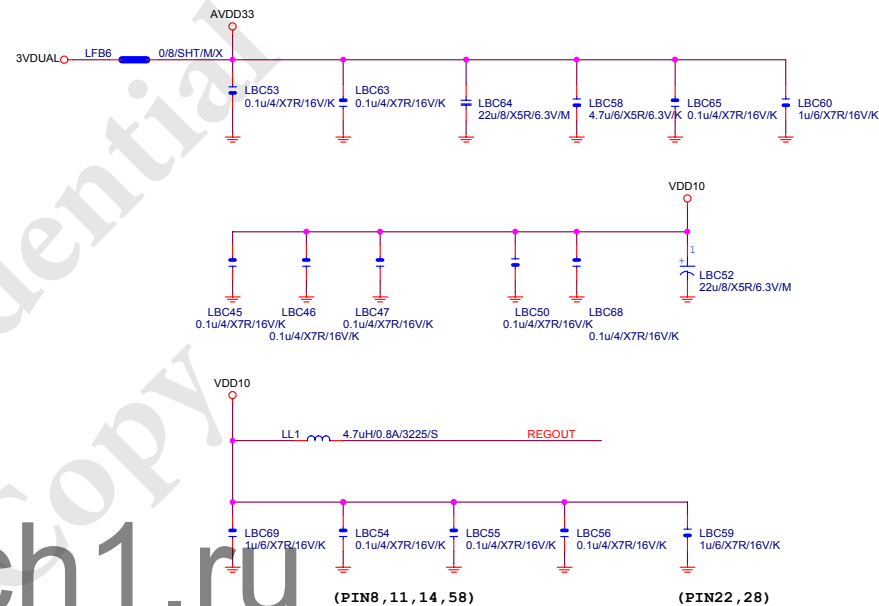
$0.6 \times (1 + 1.5K / 1K) = 1.5V$

GIGABYTE®		
DDR POWER		
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PCIE-1G LAN



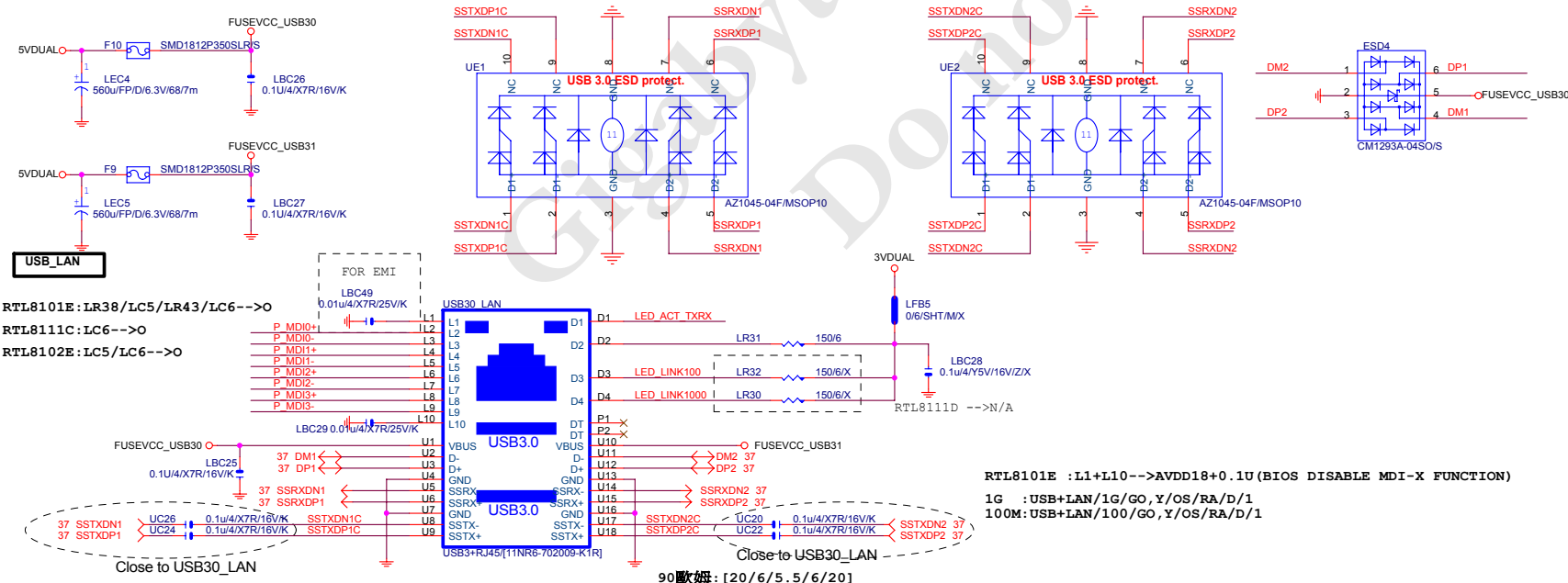
(PIN16, 37, 46, 53, 62)



(PIN8, 11, 14, 58)

(PIN22, 28)

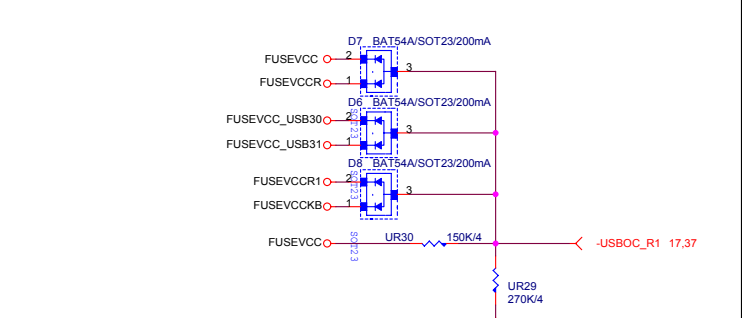
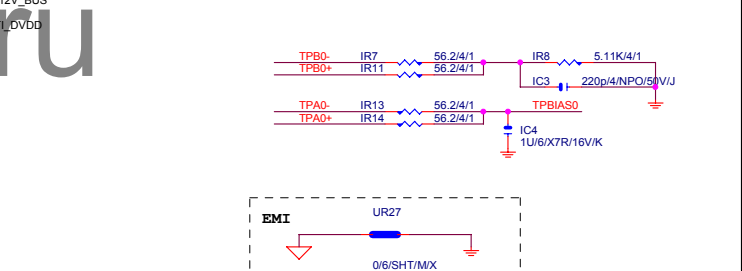
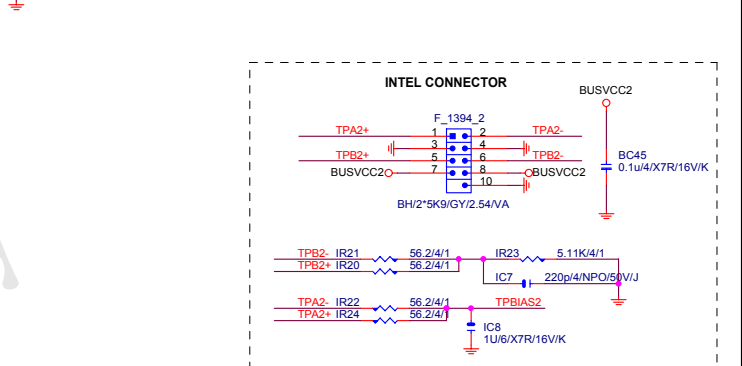
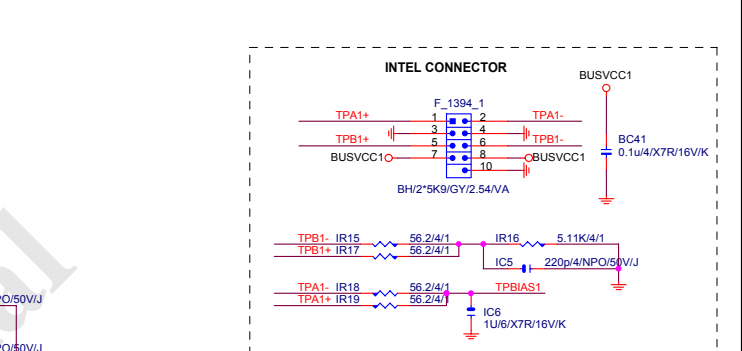
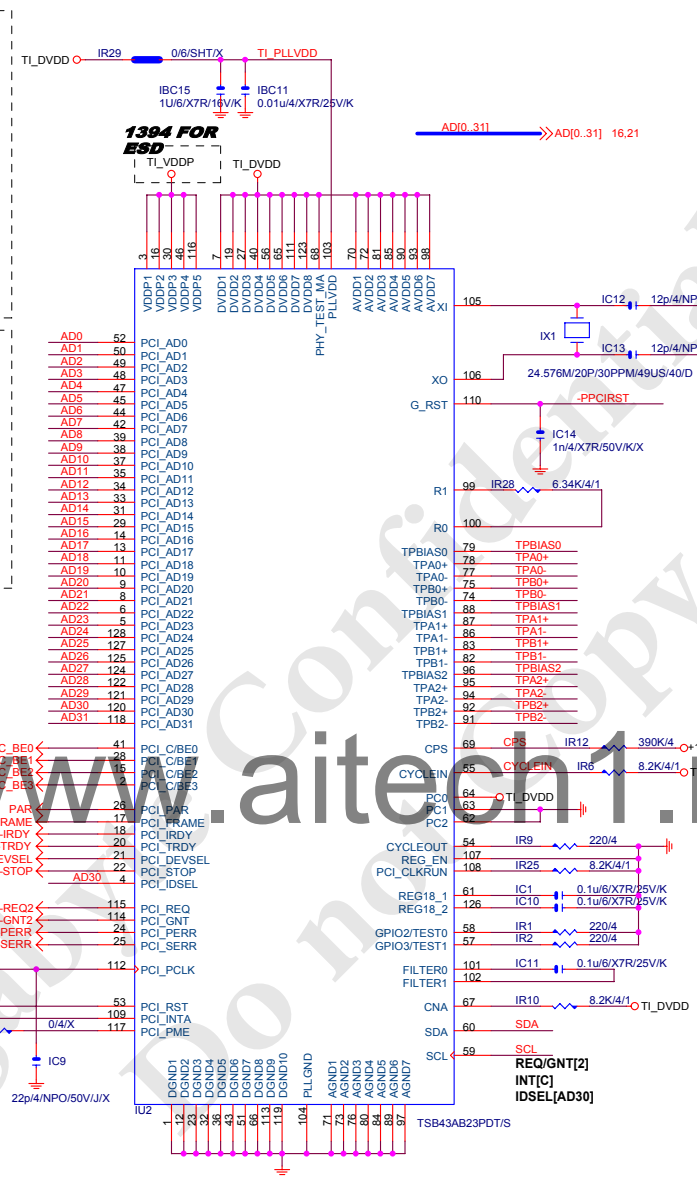
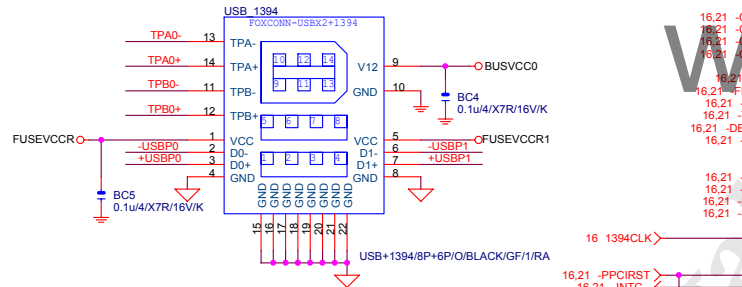
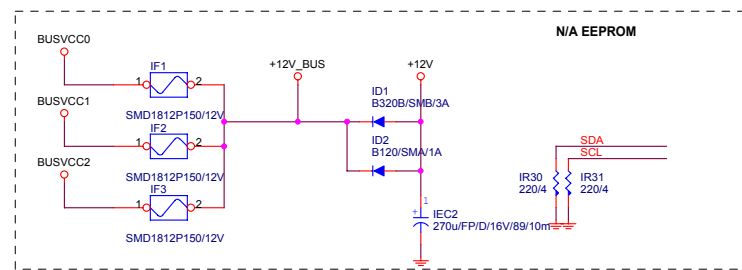
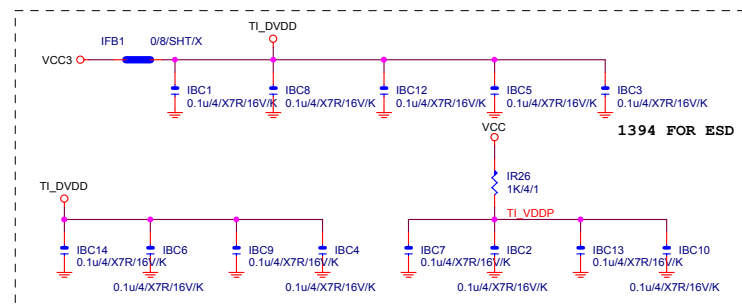
USB_LAN

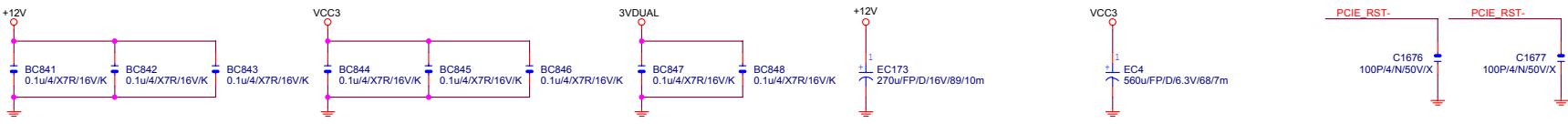
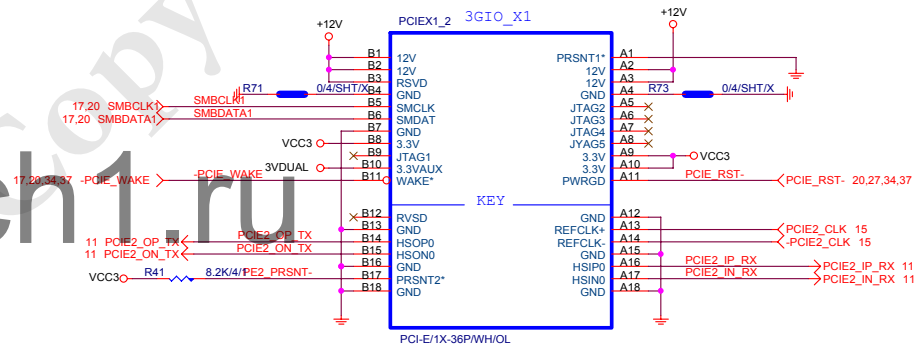
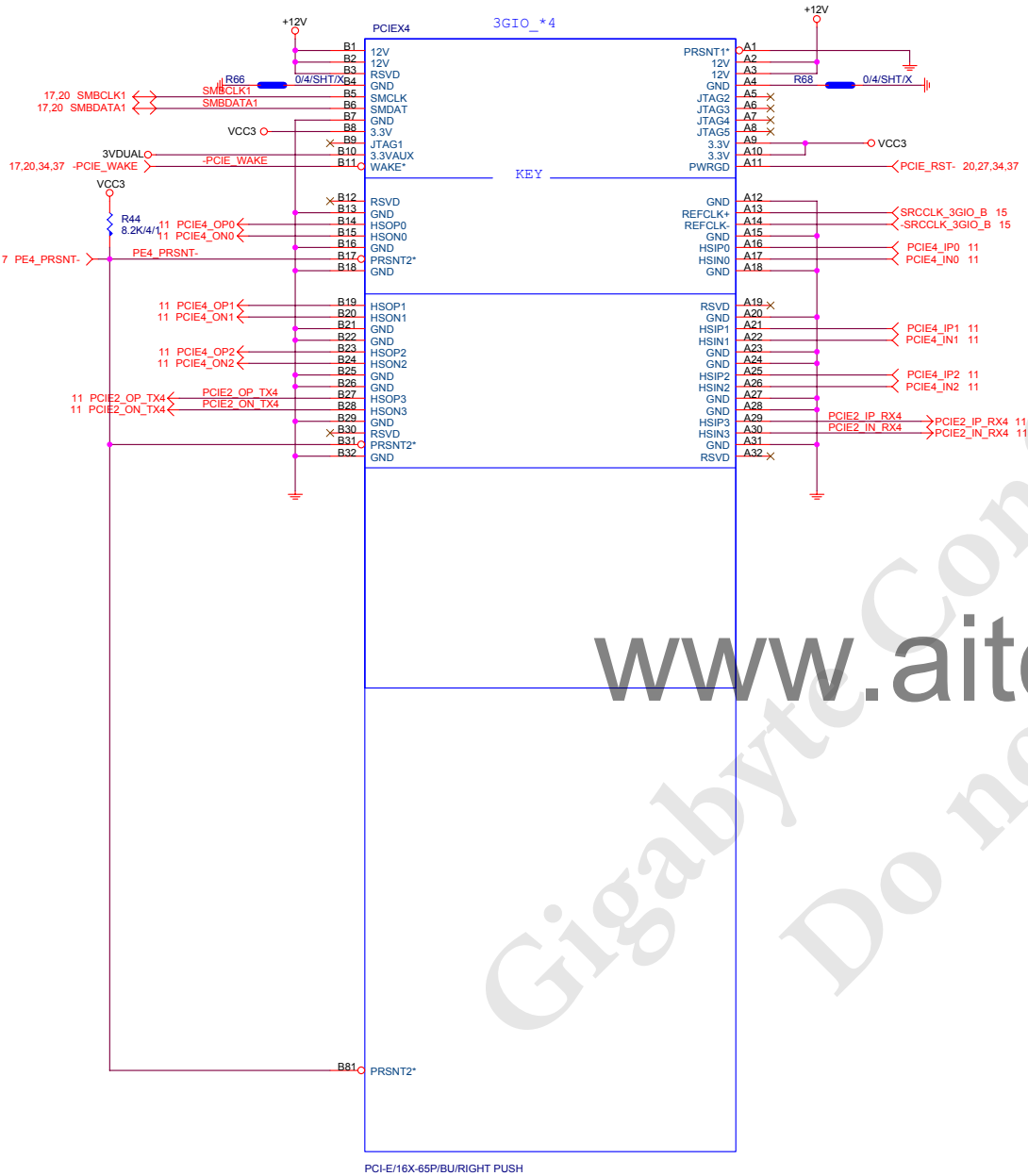


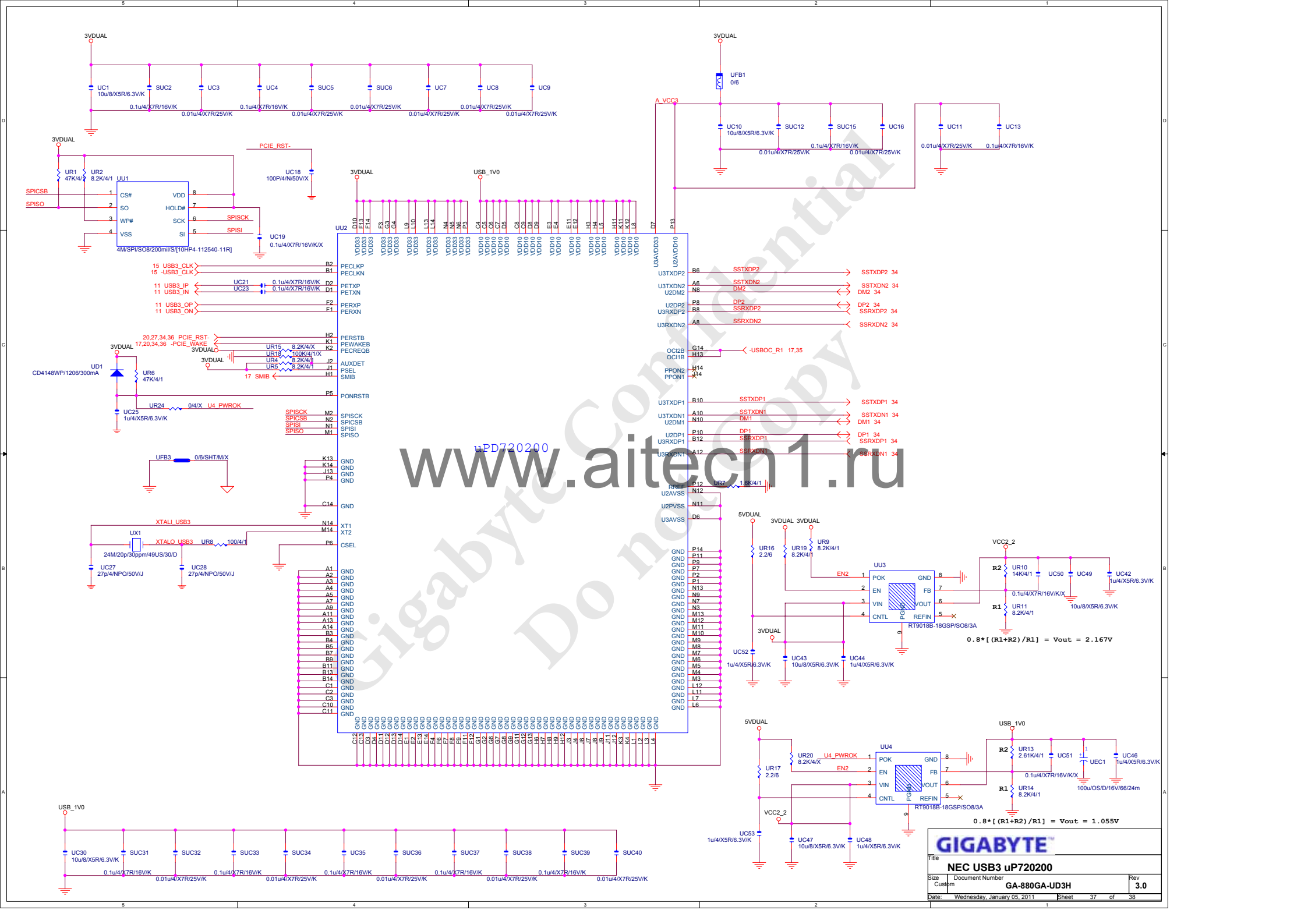
RTL8101E : L1+L10-->AVDD18+0.1U(BIOS DISABLE MDI-X FUNCTION)

1G : USB+LAN/1G/GO,Y/OS/RA/D/1
100M: USB+LAN/100/GO,Y/OS/RA/D/1

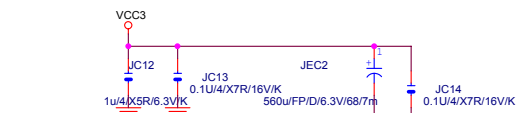
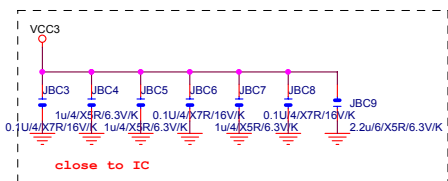
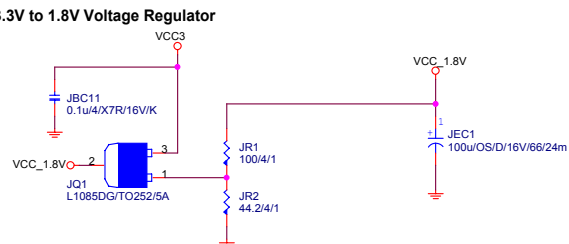
GIGABYTE®			
Title REALTK RTL8111E			
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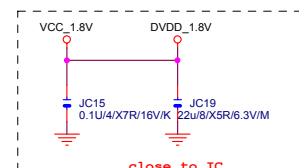




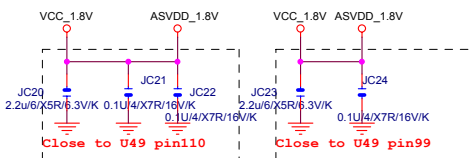
3.3V to 1.8V Voltage Regulator



Close to U49 pin94 and pin105

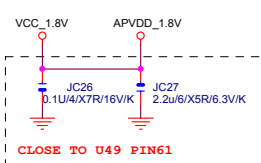


close to IC _ _

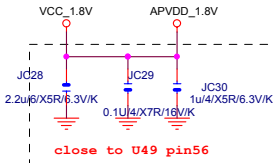


Close to U49 pin110

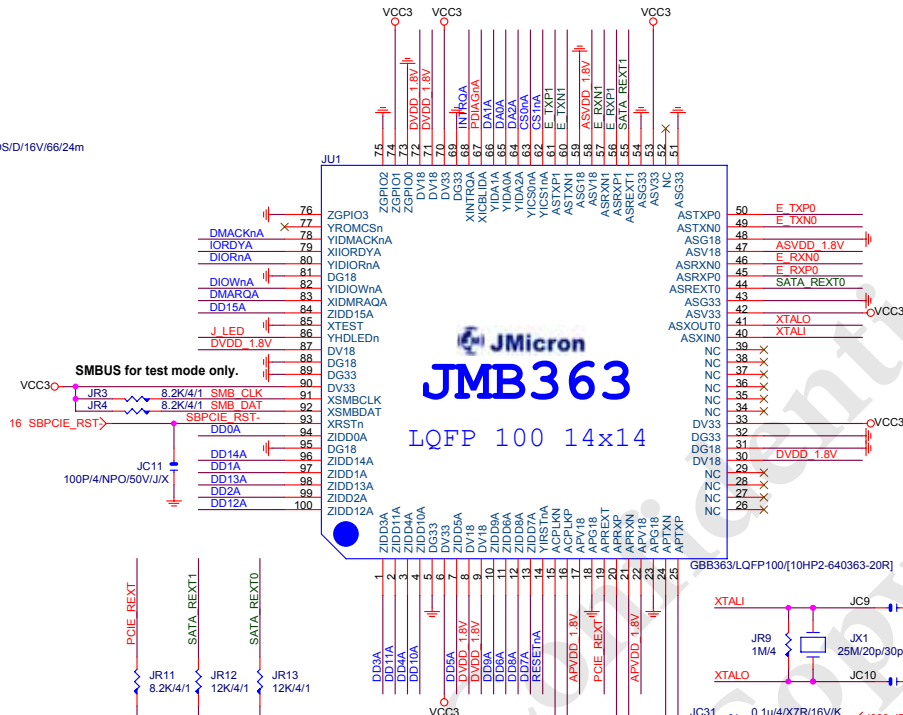
Close to U49 pi



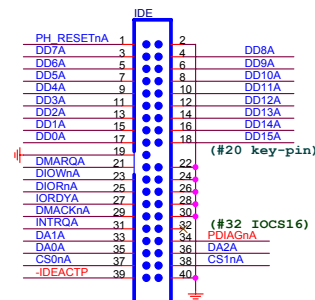
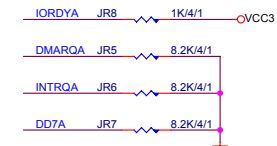
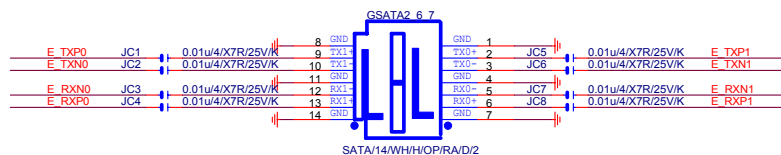
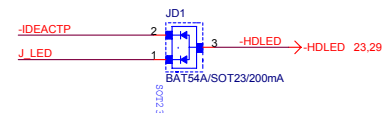
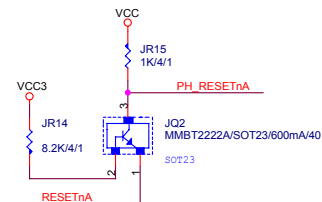
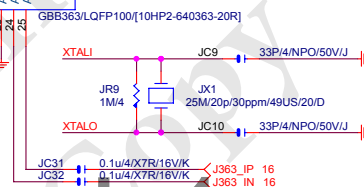
CLOSE TO U49 PIN61



close to U49 pin56



Near to PIN Check SATA eye
PCIE_REXT --> 8.06K/4/1



BH/2*20K20/WH/SHN/2.54/VA/PA46